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Effective channel length and parasitic resistance determination in non self-aligned low temperature polycrystalline silicon thin film transistors

A. Valletta [a,*], M. Rapisarda [a], L. Mariucci [a], A. Pecora [a], G. Fortunato [a], C. Caligiore [b], E. Fontana [b], F. Tramontana [b], S. Leonardi [b]

[a] CNR-IMM, via del Fosso del Cavaliere 100, 00133, Roma, Italy
[b] STMicroelectronics, Stradale Primosole 50, 95121, Catania, Italy

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ABSTRACT

The presence of high electric fields at the drain junction in polycrystalline silicon (polysilicon) thin film transistors (TFTs), enhances several undesired effects, such as hot-carrier related instabilities and kink effect. In order to reduce the drain electric field, non-self-aligned (NSA) device architecture can be adopted. In this case, dopant activation and active layer crystallization are achieved at the same time by excimer laser annealing, resulting in a substantial lateral dopant diffusion. The gradual doping profile provides not only a reduction of the drain electric field, but also a channel length shortening. Therefore, an effective channel length (L_{eff}) has to be determined in such devices, in order to successfully design circuit applications. In this work, L_{eff} and parasitic resistance (R_p) modulation effects have been investigated in both n- and p-channel NSA polysilicon TFTs. Three different parameter extraction methods, originally proposed for the crystalline MOSFETs technology, have been used and compared in order to extract L_{eff} and R_p, including: the "channel resistance" method; the "paired V_g" method; the "shift and ratio" method. These methods indicate a channel length reduction up to 1 μm and a non negligible parasitic resistance effect. The reliability of the results of the three methods are discussed in terms of applicability of the underlying assumptions in the case of polysilicon TFTs and numerical simulations are used to support the analysis.

1. Introduction

Polycrystalline silicon (polysilicon) thin film transistor (TFT) technology is emerging as a key technology for both active matrix liquid crystal displays (AMLCDs) [1] and active matrix organic light emitting displays (AMOLEDs) [2], allowing the integration of both active matrix and driving circuitry on the same substrate. Conventional polysilicon TFTs are fabricated according to the self-aligned architecture, that, due to abruptness of the lateral n^+ doping profile in the drain, present several undesirable effects in the electrical characteristics, including large off-current [3], kink-effect [4] and hot carrier instabilities [5]. These effects are related to the presence of high electric fields at the drain junction and, to alleviate these effects, several more advanced device structures have been investigated, including lightly doped drain (LDD) [6], drain offset [7], multiple gate [8] and Gate Overlapped LDD (GOLDD) [5]. However, to implement such drain field relief structures the device fabrication process has to be further complicated, by adding, for instance, a second ion-implantation step for GOLDD or LDD architectures. It is, therefore, desirable for low-cost high performance applications to develop new solutions for the drain contact configurations in order to reduce the electric fields while keeping the device fabrication simple.

An interesting alternative can be represented by non-self-aligned (NSA) processes [9], where due to the lateral doping profile at the source and drain contacts, induced by the laser crystallization process, the electric fields can be substantially reduced. Such profiling determines an effective channel length (L_{eff}) reduction, with respect to the nominal channel length (L_{nom}), that must be taken in account in order to successfully model the electrical behaviour of these devices, especially for short channel lengths.

In the present work we analyse the effective channel length and parasitic resistance of n- and p-channel NSA devices by using three different methods: the results obtained are then validated by using 2D numerical simulations.

2. Experimental

Both n- and p-channel NSA polysilicon TFTs were fabricated on oxidized silicon wafers according to a process, similar to what is already reported in the literature [10], whose main steps are: 1) a-Si film deposition, as active layer precursor, at 530 °C by LPCVD to a thickness of 100 nm; 2) for n-channel devices, n^+ source and drain region formation by a P implant dose of 2×10^{15} cm^{-2}, while for p-channel devices, p^+ source and drain region formation by a B implant

* Corresponding author. Tel.: +39 06 4993 4541; fax: +39 06 4993 4066.
E-mail address: antonio.valletta@artov.imm.cnr.it (A. Valletta).

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dose of 10^{15} cm^{-2}; 3) excimer laser irradiation, using a line beam and 40 shot/point process, to induce simultaneous crystallisation of the Si film and dopant activation; 4) gate oxide (100 nm thick) deposition by TEOS PECVD at 350 °C; 5) source, drain and gate regions metallization; 6) sintering of the metal contacts at 380 °C in forming gas. It should be pointed out that all the processing steps used are compatible with the adoption of a glass substrate, such as Corning Glass 1737, since the maximum temperature does not exceed 530 °C.

We note that by increasing the number of shots we can expect two main effects: 1) the quality of the active layer improves, since the average size of the polycrystalline grains that are obtained increases as the number of shots for point is increased [11], thus leading to a reduction in the effective density of traps in the active layer due to the reduction of grain boundary density per unit area; 2) the lateral doping profile at the source and drain region broadens, as the length of the lateral penetration, L_{lat}, roughly estimated as

$$L_{lat} = (D\tilde{n}t_{melt})^{1/2}, \quad (1)$$

where D is the diffusion coefficient of the dopant in liquid silicon and t_{melt} is the total melt duration, increases with increasing t_{melt}, which is obviously related to the number of shots.

Fig. 1a shows the transfer characteristics, normalized to the nominal channel length, measured on a set of n-channel and p-channel TFTs, with L_{nom} ranging from 3 μm to 20 μm. We note that the devices with shorter L_{nom} have normalized I_d–V_{gs} curves that lay well above those of devices with longer L_{nom}, in contrast to what found for devices with self-aligned architecture (see, for example, Fig. 1 of ref. [12]), in which the short channel curves lay below the long channel ones, due to parasitic resistance effects [12]. Moreover, also the measured normalized transconductance, $g_m \times L_{nom}$ vs gate bias, V_{gs}, (see Fig. 1b), shows that short channel TFTs have a much larger $g_m \times L_{nom}$ maximum value when compared to long channel devices, for both p- and n-channel TFTs. This behaviour can be explained by noting that the increased lateral penetration of the doping into the channel region in NSA devices tends to reduce the effective channel length (L_{eff}) and, for relatively short channel devices, L_{eff} can be appreciably shorter than the nominal channel length, L_{nom}. Thus, in such devices, L_{nom} largely overestimate the L_{eff}, leading to the observed trend in the $I_d \times L_{nom}$ and $g_m \times L_{nom}$ curves. This, of course, creates the problem to precisely determine L_{eff}, a well known problem encountered in c-Si MOSFETs [13–15].

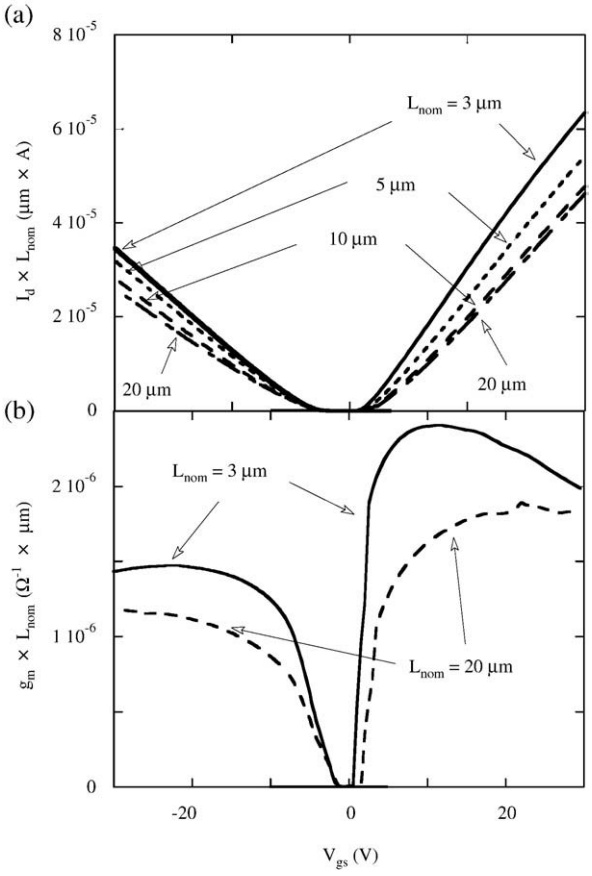

Fig. 1. Transfer characteristics normalized to the channel length (a) and corresponding transconductance (b) measured on a set of n-channel and p-channel TFTs with L_{nom} ranging from 3 μm to 20 μm. Both measurements have been normalized to L_{nom}. For clarity, only the measurements at $L_{nom} = 3$ μm and $L_{nom} = 20$ μm have been shown in panel (b). $V_{ds} = 0.1$ V in all measurements.

3. Effective channel length determination

3.1. The "channel resistance" method

In order to determine L_{eff} we applied the "channel resistance" method [16], which allows to evaluate both L_{eff} as well as the parasitic resistance from a series of transfer characteristics measurements at low drain bias on devices with different L_{nom}. In this method it is assumed that the overall device resistance (R_{tot}) is given by the sum of the effective channel resistance, ($R_{ch} \times L_{eff}$, R_{ch} being the channel resistance for unit length), and a parasitic resistance R_p. R_{ch} is supposed to be gate modulated while R_p and L_{eff} are assumed independent from the gate bias and the overall resistance is given by

$$R_{tot}\left(V_{gt}\right) = R_{ch}\left(V_{gt}\right) \times L_{eff} + R_p = R_{ch}\left(V_{gt}\right) \times L_{nom} + R_{ext}\left(V_{gt}\right), \quad (2)$$

having defined

$$R_{ext}\left(V_{gt}\right) = R_p - R_{ch}\left(V_{gt}\right) \times \Delta L \quad (3)$$

with the gate overdrive $V_{gt} = V_{gs} - V_t$, the effective channel length reduction $\Delta L = L_{nom} - L_{eff}$.

In this method it is important to group the measurements at same V_{gt}, in order to compensate for short channel effects and also for threshold voltage fluctuations from device to device, that are likely to occur in excimer laser crystallized (ELC) polysilicon [17]. In fact the polysilicon grains obtained by the ELC process are the result of a stochastic process and have dimensions and quality that can vary from grain to grain, leading to a material whose properties, such as the carrier mobility and the density of states, can slightly vary from point to point.

Following the "channel resistance" method, for a given V_{gt}, by using the linear least squares method, it is possible to determine R_{ch} (V_{gt}) and R_{ext} (V_{gt}) by fitting R_{tot} against L_{nom} as given by Eq. (2). Then, by linear fitting R_{ext} (V_{gt}) against R_{ch}(V_{gt}) (Eq. (3)), it is possible to determine R_p and ΔL and, hence the effective channel length. In Fig. 2 it is shown a typical plot of R_{tot} (V_{gt}) against L_{nom} for two (close) values of V_{gt}: even if the measurements have been made at same gate overdrive, some scattering of the data as the L_{nom} is varied is still clearly noticeable and it can be attributed to the mobility fluctuations due to the use of the ELC process: indeed, the amount of the deviation of the R_{tot} of a specific device upon the best fit line can be taken as an indicator of deviation of the carrier mobility of the device from the average mobility.

The plot of R_{ext} (V_{gt}) as a function of R_{ch}(V_{gt}) is shown in Fig. 3: from this plot it has been deduced the ΔL and R_p values shown in Table 1. As can be seen, the ΔL determined for the n-channel devices ($\Delta L_n = 1.24$ μm) (source and drain are doped with phosphorous) is higher than the ΔL determined for the p-channel devices ($\Delta L_p = 0.77$ μm) (with source and drain doped with boron). The reason for this difference can be attributed to the difference of the