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Solid phase epitaxy on N-type polysilicon films formed by aluminium induced crystallization of amorphous silicon

Ö. Tüzün [a,*], A. Slaoui [a], S. Roques [a], A. Focsa [a], F. Jomard [b], D. Ballutaud [b]

[a] InESS, UMR 7163 CNRS-UdS, 23 rue du Loess, F-67037 Strasbourg Cedex 2, France
[b] GEMaC-UMR 8635 CNRS, 1 place Aristide Briand, F-92195 Meudon, France

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ABSTRACT

In this work, undoped amorphous silicon layers were deposited on n-type AIC seed films and then annealed at different temperatures for epitaxial growth. The epitaxy was carried out using halogen lamps (rapid thermal process or RTP) or a tube conventional furnace (CTP). We investigated the morphology of the resulting 2 μm thick epi-layers by means of optical microscopy. An average grain size of about 40 μm is formed after 90 s annealing at 1000 °C in RTP. The stress and degree of crystallinity of the epi-layers were studied by micro-Raman Spectroscopy and UV–visible spectrometer as a function of annealing time. The presence of compressive stress is observed from the peak position which shifts from 520.0 cm^{-1} to 521.0 cm^{-1} and 522.3 cm^{-1} after CTP annealing for 10 min and 90 min, respectively. It is shown that the full width at half maximum (FWHM) varies from 9.8 cm^{-1} to 15.6 cm^{-1}, and the magnitude of stress is changing from 325 MPa to 650 MPa. Finally, the highest crystallinity is achieved after annealing at 1000 °C for 90 min in a tube furnace exhibiting a crystalline fraction of 81.5%. X-ray diffraction technique was used to determine the preferential orientation of the poly-Si thin films formed by SPE technique on n^+ type AIC layer. The preferential orientation is ⟨100⟩ for all annealing times at 1000 °C.

1. Introduction

Polycrystalline silicon (poly-Si) thin films on foreign substrates (such as glass, alumina, mullite) are an interesting alternative technology to traditional bulk Si solar cells. Relatively large grain size, in the range 1 μm to 1 mm [1], crystalline fraction close to 100%, and low-cost fabrication are the main advantages of the polycrystalline silicon thin films. There are various techniques for the formation of polycrystalline silicon on foreign substrate. Solid phase crystallization (SPC) of amorphous silicon (a-Si) is a way for the high-efficiency poly-Si based cells with 9.2% efficiency [2]. The drawbacks of SPC are however long thermal process (days), small grain size (1–2 μm) and poor crystallographic properties [3]. On the other hand, the polysilicon seed layer can be an alternative approach. It consists in forming the polysilicon layer using a low thermal budget method and then thickening it by means of an epitaxy process [4]. The aluminium induced crystallization (AIC) technique has been reported to form the seed poly-Si layer [5]. For the formation of the active layer, different methods can be used such high temperature CVD, ion assisted deposition (IAD), low temperature ECR-PECVD as well as solid phase epitaxy (SPE). On the other hand, fabrication of n-type poly-Si solar cells is suited for many reasons [6] such as higher lifetime and diffusion length [7] and less recombination at grain boundaries and surface defects [8]. More importantly, the SPE is also expected to be enhanced on n-type seed layer and larger grain sizes [9] are expected. However, few investigations concerned the solid phase epitaxy (SPE) [3] of a-Si deposited on n-type polysilicon layers by means of conventional or rapid thermal annealing using halogen lamps.

In this paper, we investigate the formation of a n^+–n polysilicon structure by combining the AIC and SPE processes. Thus the p-type AIC layer is first transformed into a n^+ polysilicon seed film by thermal diffusion of phosphorus from a solid source spun onto the AIC seed layer. Then the SPE technique that consists of a-Si deposition by ECR-PECVD and ex situ annealing for the crystallization using a rapid thermal process (RTP) or a classical thermal process (CTP) is used to thicken the seed layer. The n-region is formed during the ex situ annealing by exodiffusion from the n^+ seed layer into the epi-layer. The resulting n^+–n structure is analyzed in terms of crystallographic properties and surface morphology. An optical microscope was used for this purpose. The stress and degree of crystallinity of the epi-layers were studied by the micro-Raman Spectroscopy and UV–visible spectrometer. The preferential orientation of the resulting n-type epi-layer is deduced from the X-ray diffraction technique.

2. Experimental

Alumina (Al_2O_3) was used as a substrate. Flowable oxide (FOx-25 from Dow Corning) that contains Hydrogen Silsesquioxane Resin HSQ:

* Corresponding author. Tel.: +33 388 10 6332; fax: +33 388 10 6335.
E-mail address: Ozge.Tuzun@iness.c-strasbourg.fr (Ö. Tüzün).

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Table 1
Full width at half maximum (FWHM) as deduced from Raman spectroscopy measurements on epi-layer polysilicon formed by conventional thermal annealing of a-Si on n^+ seed Si layer.

Annealing temperature (°C) (CTP)	700	800	900	1000
FWHM (cm^{-1})	15.6	13.7	11.7	9.8

$(HSiO_{3/2})_n$ was spun onto the alumina. FOx smoothed extremely rough alumina surface and behaves as a barrier between alumina and Si layers. The effect of FOx on rough alumina surface was discussed in previous paper [10]. FOx coating on alumina substrates were followed by the AIC process to produce ~200 nm thick poly-Si seed layer. AIC process includes respective Al and a-Si depositions. 200 nm thick Al was deposited by electron beam evaporation system. Prior to a-Si deposition the samples were exposed to ambient air for one week to form aluminium oxide layer (AlO_x) which behaves as a permeable membrane separating the Al and a-Si layers during the AIC exchange process. It has been extensively shown that this layer controls the diffusion of silicon into the aluminium [11,12]. Then 370 nm thick a-Si was deposited by ECR-PECVD at deposition rate of 3.7 Å/s. After the a-Si deposition, Al_2O_3/FOx/Al/AlO_x/a–Si structures were annealed at 500 °C for 5 h under nitrogen flow to complete the formation of the AIC layer by the layers' exchange process. After the exchange, a residual layer consisting of Al + Si islands remains on top of the AIC layer [13]. This residual layer was cleaned by the chemical etching.

AIC process was followed by the overdoping of phosphorus solution. Highly phosphorus doped glass solution (P505 from Filmtronics Inc.) was spun onto the surface and baked at 80 °C for 5 min and at 200 °C for 10 min in order to remove the solvents. The phosphorus concentration of the P505 solution is 4.5×10^{19} at cm^{-3}. The samples were then annealed in a tube furnace at 1000 °C for 1 h under argon flow for the diffusion of phosphorus into the poly-Si seed layer. The residual phosphorus oxide layer on top was cleaned by HF (5%).

ECR-PECVD system was used for depositing intrinsic a-Si layer for SPE to thicken the AIC seed layer. The SiH_4/Ar mixture gas was fed into ECR-PECVD. Gas flow rates used were 15 sccm of argon (Ar) as carrier gas and 10 sccm of silane (SiH_4) as precursor gas. SPE was performed at 250 °C. The total pressure during a-Si deposition was about 5.2 mTorr and the microwave power was about 500 W. By using these deposition conditions 2 μm thick films of a-Si were deposited on n^+ type poly-Si. After a-Si deposition, SPE crystallization and exodiffusion anneals were performed ex situ in rapid thermal process (RTP) or classical thermal furnaces (CTP) under pure argon flow. The temperature range was from 700 °C to 1000 °C for CTP process while 1000 °C was used as the annealing temperature for RTP.

Poly-Si thin films with different anneal conditions were structurally investigated by optical microscope, micro-Raman spectroscopy, X-ray diffraction and UV/Vis/NIR reflectance spectroscopy. The optical microscope is a Leica DM-LM equipped with a 100 W halogen illumination and a Canon S40 video camera mounted on the auxiliary port. It is interfaced to a computer for data storage and data processing. The Raman spectra were obtained on a Renishaw RAMASCOPE 2000 μ-Raman spectrometer with the 488 nm excitation wavelength of an Ar^+ laser. The crystallographic structure of the samples was checked at room temperature using a Siemens D-5000 X-ray powder diffractometer with monochromatic CuKα_1 incident beam ($\lambda = 0.154056$ nm) operated at 35 kV and 25 mA. The samples were scanned for a range of 2θ from 20° to 90° in the symmetric diffraction mode for analysis of the film bulk, and in the asymmetric mode (glancing incidence of 5°) for more surface-sensitive characterization. Optical reflectance spectra of poly-Si thin films were obtained using a Perkin Elmer Lambda 19 UV/Vis/NIR spectrometer within the range 200–1200 nm wavelength range.

3. Results and discussions

As described in the experimental part, the temperature range for CTP was from 700 °C to 1100 °C while 1000 °C was used as the annealing temperature for RTP. But according to the full width at half maximum (FWHM) of Raman peak that indicates the best crystallinity of the samples (i.e. the lowest FWHM) was reached at 1000 °C for CTP as shown in Table 1. Therefore, 1000 °C was used as the crystallization temperature in CTP later on. However the annealing time was used as a parameter.

3.1. Optical microscope analysis

Fig. 1a and b present the optical microscope (OM) images of n^+–n type poly-Si structures after recrystallization at 1000 °C in RTP and CTP furnaces, respectively. Also, the average grain size, as deduced from the OM images, vs. annealing time for both annealing processes is plotted in Fig. 2. Poly-Si layers with grain structure were obtained after the crystallization annealing. The crystallization in few seconds for RTP treatment can be explained by the incubation time. RTP decrease the incubation time, so a-Si with RTP starts nucleation for short times [14,15]. As a result, the crystallization can be completed in fewer annealing time with large grain sizes. Fig. 2 indicates that the poly-Si grain sizes increases with the longer annealing times for either RTP or CTP. Thus quite large grains up to values of the order of ~40 μm are obtained by using SPE on n^+ type poly-Si. More importantly, less defective surface (Fig. 1) and larger (average) grain sizes (Fig. 2) are obtained after RTP. Clearly, low thermal budget for RTP treatment is very promising to obtain higher quality polycrystalline silicon when

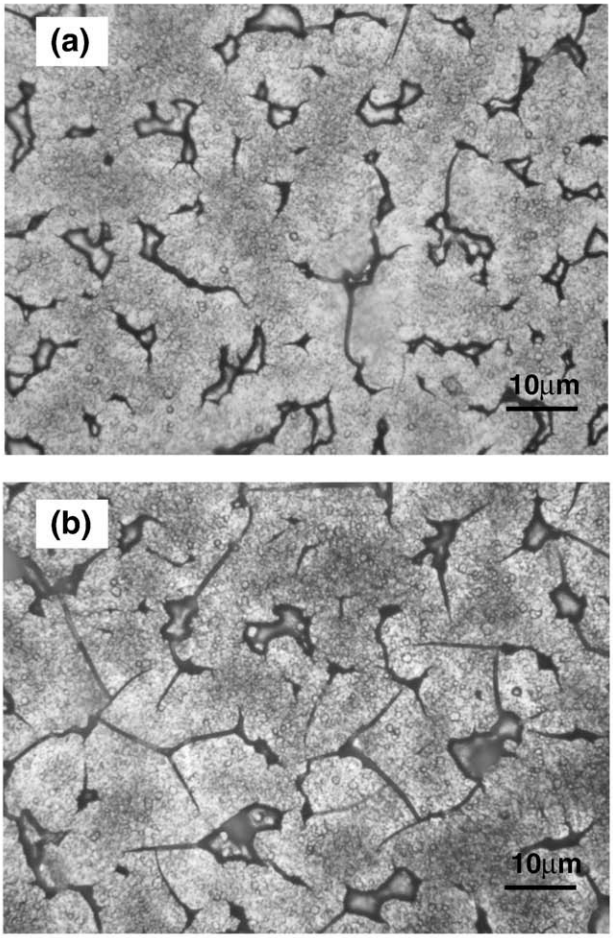

Fig. 1. Optical microscope images showing the surface morphology: (a) in CTP at 1000 °C for 30 min, and (b) in RTP at 1000 °C for 30 s.