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Electronic and structural properties of the amorphous/crystalline silicon interface

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ABSTRACT

A review of capacitance and conductance measurements on (n) a-Si:H/(p) c-Si structures is presented. Capacitance measurements performed on cells under AM 1.5 illumination at or close to open-circuit voltage are sensitive to the recombination at interfaces, as evidenced by the comparison with photoluminescence results. Capacitance measurements performed in the dark at zero or reverse bias can reveal the presence of interface defects from trapping and release of carriers, but the sensitivity is limited to a few 10^{12} cm^{-2} eV^{-1}. This is partly due to the presence of a strong inversion layer at the c-Si surface. Such a layer has been revealed from coplanar conductance measurements, which allow a precise determination of the conduction band offset, found equal to 0.15 ($\pm$0.04) eV. As shown by spectroscopic ellipsometry, a thin undoped silicon layer deposited under conditions that normally produce polymorphous silicon can be epitaxially grown onto c-Si prior to the (n) a-Si:H layer. Electrical measurements indicate that this additional buffer layer is not detrimental and can slightly improve the interface quality.

1. Introduction

Silicon heterojunction solar cells combining crystalline and thin film silicon technologies are attracting much interest. This is because very high efficiencies (above 22%) have been demonstrated, while, from a technical point of view, the energy consumption and cost effective processing steps used to form the junctions or back surface field in the traditional crystalline solar cell fabrication are replaced with the low temperature processing steps of silicon thin film deposition [1]. Thanks to the use of various characterization techniques some physical aspects of the heterojunction between hydrogenated amorphous silicon (a-Si:H) and crystalline silicon (c-Si) have been clarified, and significant improvements in solar cell performance have been obtained in the past few years [2–8]. However, there is still a number of interface related issues that need to be investigated. We here give a summary of characterization results obtained on (n) a-Si:H/(p) c-Si interfaces using a set of both electrical and optical techniques: capacitance and conductance measurements, spectroscopic ellipsometry, and photoluminescence. We emphasize the potentialities and limits of these techniques for the determination of interface parameters such as interface defect densities, capture cross sections, and band offsets. Finally, we address the role of the so-called "intrinsic" buffer layer, and discuss its amorphous or crystalline nature related to possible epitaxial growth.

2. Experimental details

Two types of solar cells based on p-type c-Si were fabricated on flat Czochralski c-Si wafers (<100> oriented, p-type, $\rho = 14$–$22\ \Omega$ cm) and analysed. Single heterojunction solar cells have an aluminium (Al) back surface field, while double heterojunction solar cells have a back interface consisting of a (p) c-Si/(p) a-Si:H heterojunction (Fig. 1). In both types of solar cells, the front emitter consists of an (n) a-Si:H layer deposited by rf PECVD (13.56 MHz) from a silane–phosphine mixture at a pressure of 50 mTorr, power density of 6 mW/cm^2, and substrate temperature of 200 °C. Before the thin-film deposition, the c-Si surface was prepared by removing the native oxide using a wet chemical etching procedure (HF diluted at 5% in DI water). The influence of an additional undoped buffer layer between a-Si:H and c-Si was also studied. This buffer layer was deposited under conditions that normally lead to undoped hydrogenated polymorphous silicon ((i) pm-Si:H) when deposition is made on glass, namely from a silane–hydrogen mixture at a pressure of 1200 mTorr, power density of 23 mW/cm^2, and substrate temperature of 200 °C. We will show in Section 4 that this layer is actually epitaxially grown onto the c-Si substrate.

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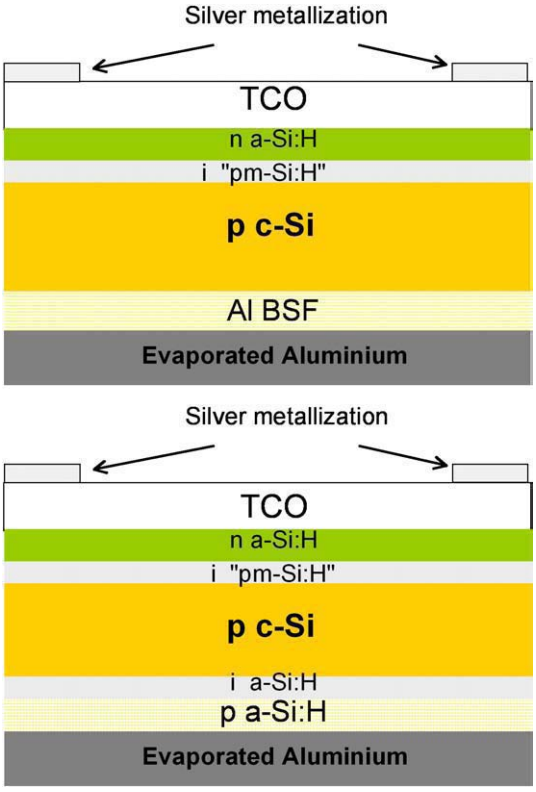

Fig. 1. Schematic view of our single (top) and double (bottom) heterojunction solar cells.

Capacitance measurements were performed on solar cells in two different regimes [9,10], using an HP4284A impedance meter in the frequency range of 100 Hz–1 MHz, with an ac measurement signal of 20 mV. Measurements in the dark at zero bias as a function of frequency and temperature $C(f, T)$ were performed in a cryostat dynamically pumped down to 10^{-5} mbar and in a wide temperature range [100 K–350 K]. Measurements under AM1.5D illumination at forward bias close to the open-circuit voltage, V_{oc}, were performed in air at 300 K.

Photoluminescence measurements were performed on symmetrical wafer structures, for which the thin-film layer sequence of the front side of the cell (emitter stack) was deposited on either side of the c-Si wafer. The samples were excited by a laser diode at a wavelength of 850 nm. The luminescence radiation was detected after dispersion by a monochromator by a liquid-nitrogen cooled InGaAs photodiode. The set-up also allows the measurement of the absolute emitted spectral photon flux density for the determination of the quasi-Fermi level splitting [11].

Conductance measurements were performed on samples consisting of (n) a-Si:H layers fitted with top coplanar Al electrodes [12]. These layers were deposited in the same run on three types of substrates: glass (Corning 1737), Czochralski c-Si wafers (<100> oriented, p-type, $\rho = 14$–$22\ \Omega$ cm), and Float Zone c-Si wafers (<100> oriented, p-type, $\rho = 1$–$5\ \Omega$ cm). Samples with an inserted undoped "pm-Si:H" buffer layer were also fabricated. The thickness of the "pm-Si:H" layer was set at 3 nm, while the thickness of the (n) a-Si:H layer was varied between 20 nm and 200 nm. Since a linear relationship was found between the dc current, I, and dc applied voltage, V, the sample conductance, G, was calculated as the ratio I/V. Measurements were performed in the same conditions as the dark capacitance measurements.

Finally, spectroscopic ellipsometry measurements were performed on these samples to study the growth of the very thin films on crystalline silicon. From these measurements, one can deduce the pseudo-dielectric function $\langle\varepsilon_1\rangle + i\langle\varepsilon_2\rangle$ which is related to the film thickness and optical properties [13]. These data have proved to be efficient in monitoring and controlling the deposition process in a-Si:H/c-Si heterojunctions, in analyzing the layer thicknesses and determining the nature (amorphous or epitaxially grown) of the layer [14,15].

3. Results and discussion

Capacitance data obtained at zero dc bias in the dark are presented in Fig. 2 for single heterojunction solar cells. For the lower quality solar cell (having a conversion efficiency of 12%) with non-optimized front emitter, we observe a capacitance step that is shifted along the temperature axis when the measurement frequency is changed. This is the typical signature of trapping and release processes from defects detected in the so-called space charge spectroscopy [16]. However, such a capacitance step is not observed for the higher quality solar cell (with an efficiency of 16%) obtained after interface optimization. The occurrence of a capacitance step and its dependence with the interface defect density has been analysed in preceding papers [9,17,18]. It has been shown that such a capacitance step is only visible for interface defect densities higher than a few 10^{12} cm^{-2} eV^{-1}. This means that detection of interface defects from the usual space charge spectroscopy technique is much poorer on a-Si:H/c-Si heterojunction solar cells compared to insulator/c-Si interfaces, where values below 10^{10} cm^{-2} eV^{-1} can be detected. This poorer detection limit is related to the peculiar band diagram of the (n) a-Si:H/(p) c-Si interface that is described in Fig. 3. First, it must be stated that in the heterojunction device interface states can exchange either electrons with a-Si:H or holes with c-Si, while in the case of the insulator/c-Si interface exchanges are only possible with c-Si since the insulator cannot provide free carriers. Exchanges of electrons at the interface will add a contribution to the a-Si:H depletion capacitance, which is much higher than the c-Si depletion capacitance. These two capacitances being in series, the sensitivity to the exchange of electrons will be very poor. Exchanges of holes at the interface will add a contribution to the c-Si depletion capacitance, which is indeed directly reflected in the total capacitance. So, only the exchange of holes at the interface can produce a strong capacitance step in the $C(T)$ curve. However, if the density of interface states is low enough that it does not modify the band diagram compared to the ideal band diagram without interface states, it can be seen from Fig. 3 that the strong band bending imposed by the heterojunction produces a strong inversion layer at the c-Si surface. The interface Fermi level is then very close to the conduction

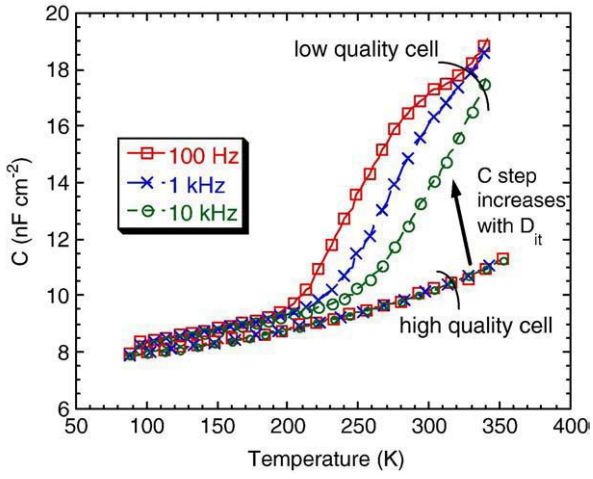

Fig. 2. Zero bias capacitance measured on two solar cells in the dark as a function of temperature at three frequencies. The capacitance step is not visible on the best cell (for which the defect density at the emitter interface, D_{it}, is below 5×10^{12} cm^{-2} eV^{-1}). It increases when D_{it} increases.