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Effect of gate insulating layer on organic static induction transistor characteristics

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ABSTRACT

Organic static induction transistors, which have relatively short vertical channels, are attractive devices for their low operating voltage and high operating speed. However, a gate voltage larger than the Schottky barrier potential usually leads to a large gate leakage current and thus poor device performance. To limit the gate leakage current, we considered adding insulating layers around the gate electrode. The oxidization of aluminum during a physical vapor deposition process was used to form insulating layers around the gate electrode. The results demonstrate that by appending gate insulating layers, gate leakage currents can be effectively reduced and device characteristics, especially the on/off ratio, can be improved.

1. Introduction

Recently, the promising applications of organic electronics in large area, low cost and flexible electronic products are attracting more and more attention [1,2]. However, problems such as low carrier mobility, high resistivity and instability of organic materials still remain. To solve these problems, researchers have been putting enormous effort in synthesizing materials, improving device structures or developing new process technologies [3–5]. In the field of organic transistors, thin film transistor (TFT), which is well adapted to low conductivity materials, is the main adopted structure. In addition, inorganic TFT theory is widely used in organic lateral-channel transistors, namely, organic field-effect transistors (OFETs) [6,7]. However, a gate voltage as high as several ten volts is usually necessary to form an accumulation layer at the interface between the gate insulator and the organic semiconductor. A poor frequency response will be caused due to the low current density and the capacitance between the electrodes. Therefore, practical applications of OFETs are still difficult. One reason for the poor performance of OFETs is the channel length, which is usually as long as several micrometers. However, it is not easy to obtain a short channel due to the limits of fabrication technologies. On the other hand, the film thickness in an OFET is usually in the range of several ten nanometers to several hundred nanometers. Therefore, a smaller channel length can be obtained, if the channel can be established in the vertical direction [8]. From this point of view, organic static induction transistor (OSIT) with a slit-type gate electrode was proposed as a vertical type transistor [9]. Relatively high-current, high-speed and low-voltage operation was obtained in such a kind of device [10]. Further discussions on source electrodes show that controlling the interface between the source electrode and the organic semiconductor in such a kind of device has a great effect on the carrier injection barrier and thus the device characteristics [11,12]. However, as gate modulation is mainly based on the Schottky contact between the gate electrode and the organic semiconductor [8], the applicable gate voltage depends on the Schottky barrier potential. Actually, the voltage range is limited by the forward bias current of the formed Schottky diode. This means large gate current will occur when the gate voltage is beyond the barrier potential. Several groups reported that covering gate electrodes with insulating layers showed some effect on restraining leakage current in vertical type transistors [13,14]. In this research, we focused on the reduction of gate leakage current in slit-type gate OSITs and tried appending insulating layers around the gate electrodes.

2. Experimental details

Fig. 1(a) shows the structure of conventional OSITs we fabricated. An indium tin oxide (ITO) patterned glass plate was employed as the substrate, where the 100 nm thick ITO served as the source electrode. Both the gate electrode and the drain electrode were formed with aluminum (Al). Copper phthalocyanine (CuPc), which can form a typical Schottky contact with Al, was used as the organic semiconductor. All the films were made using the method of physical vapor deposition. The fabrication sequence is as follows. Before the deposition, the substrate was cleaned by ultrasonic bath (in a sequence of pure water, acetone and isopropanol at 50 °C for 10 min respectively) and UV/Ozone cleaning (at 50 °C for 5 min). Then, the first CuPc layer with a thickness of 100 nm was deposited. A slit-type mask with line/space of 20 μm/20 μm was used to form the slit-type gate electrode. By inserting a 0.5 mm thick spacer between the mask and the substrate, narrower gate gaps can be obtained on the substrate due to the additional flying room made by the

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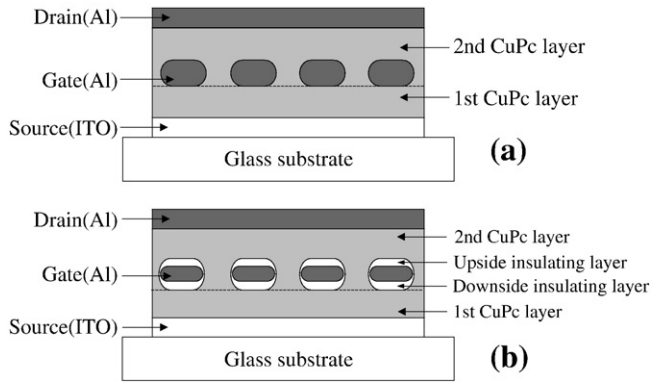

Fig. 1. OSIT structure (a) without insulating layer (b) with both sides insulating layers.

spacer for the vapor, as shown in Fig. 2. The deposition source consisted of a pyrolytic boron nitride (PBN) crucible with Al grains in it and a tungsten heater winding around the crucible. The distance between the substrate and the top of the crucible was 15 cm. More details are shown in Fig. 2. The thickness of the gate was about 20 nm. The 150 nm thick second CuPc layer was then deposited, covering the gate electrode. Finally, the Al drain electrode with 30 nm in thickness was made to complete the device. The deposition was carried out under a pressure of 5×10^{-4} Pa, with deposition rates of 0.1 nm/s and 0.5 nm/s for CuPc and Al, respectively. The effective device area was about 4 mm^2.

We found that when Al was deposited at a low rate under a relatively low vacuum condition (~10^{-3} Pa), the Al layer could be oxidized easily during the deposition. This phenomenon was used to form insulating layers around the gate electrode in our experiments. The insulating layers were fabricated under 2×10^{-3} Pa and at a rate of 0.05 nm/s and they could be of either one side or both sides. Those on the side close to the drain electrode are called upside insulating layers and downside insulating layers for those on the side close to the source electrode, as shown in Fig. 1(b). All the thicknesses of the insulating layers were evaluated with a crystal thickness monitoring system and confirmed with a high precision profilometer. The characteristics were measured with the system shown in Fig. 3, where the source electrode was set to common and variable voltages were applied to the other two electrodes. All of the measurements were carried out in air, at room temperature and under dark conditions.

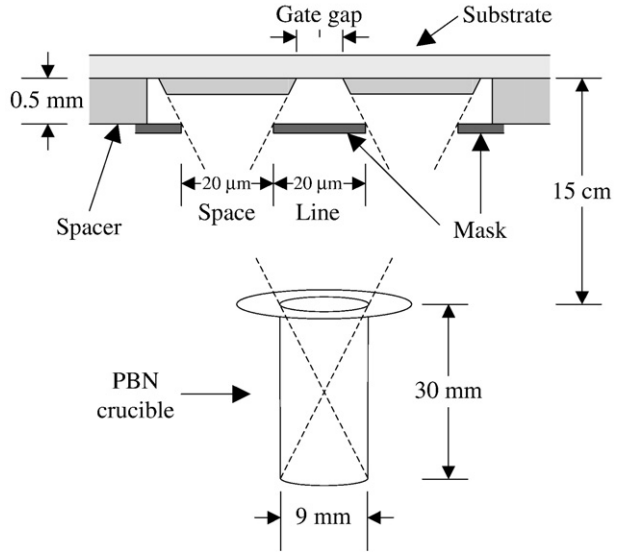

Fig. 2. Evaporation process.

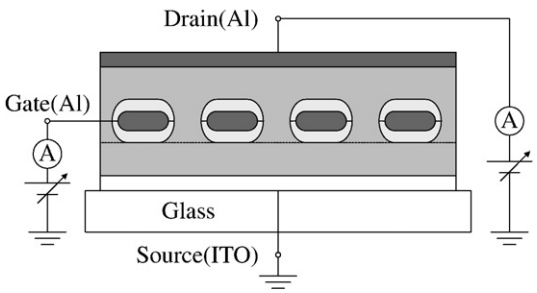

Fig. 3. Measurement system for static characteristics.

3. Results and discussion

By making use of the oxidization of Al, gate insulating layers were fabricated without causing large damage to the organic semiconductor. The layers showed good insulating properties, and the effects of these layers were investigated in three parts, as follows.

3.1. Insulativity of insulating layers

The insulating properties of the oxidized Al layers were confirmed with a sample illustrated in Fig. 4. The 200 nm thick insulating layer, which was deposited at 0.05 nm/s under a pressure of about 2×10^{-3} Pa, was sandwiched between two Al electrodes. The results indicate that the current flowing through the insulating layer in a voltage range of −5 V to 5 V was limited in a range far smaller than nanoampere order. Considering gate voltage is usually lower than 5 V and drain-source current is at least in the order of nanoampere for an OSIT, it is feasible to use such kinds of insulating layers.

3.2. Gate–drain current with source floated

The gate–drain currents in the case of no insulating layer (bare) and both sides (50 nm for downside, 30 nm for upside) are shown in Fig. 5, where the source electrode of each device is floated. The results show that whether there are insulating layers around the gate electrode or not, there is no obvious change in gate–drain current and the currents are kept in the order of several nanoamperes. This can be attributed to the double Schottky effect formed in the Al (Gate)-CuPc-Al (Drain) structure.

3.3. Gate–source current with drain floated

Fig. 6 shows the comparison of gate–source currents with drain electrodes floated among the OSITs with no insulating layer (bare), only upside insulating layer, only downside insulating layer and both

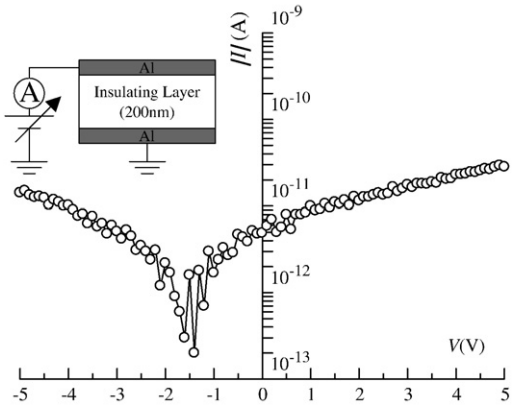

Fig. 4. *I–V* characteristics of insulating layer.