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Silicon nanocrystals synthesized by electron-beam co-evaporation method and their application for nonvolatile memory

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ABSTRACT

In this paper, the silicon nanocrystals (Si NCs)/SiO_2 hybrid films designed for nonvolatile memory applications are prepared by electron-beam co-evaporation of Si and SiO_2. Transmission electron microscopy images and Raman spectra verify the formation of Si NCs. Metal-oxide-semiconductor capacitor structure with Si NCs embedded in the gate oxide is fabricated to characterize the memory behaviors. High-frequency capacitance–voltage and capacitance–time measurements further demonstrate the memory effect of the structure resulting from the charging or discharging behaviors of Si NCs. It is found that the memory window can be changed by adjusting the Si/SiO_2 wt. ratio in source material. The memory devices with Si NCs/SiO_2 hybrid film as floating gate yield good retention characteristics with small charge loss.

1. Introduction

In order to overcome scaling down limitations of conventional nonvolatile memory (NVM), silicon nanocrystal (Si NC) floating gate memories have recently attracted extensive attention [1,2], due to their promising characteristics, for example, compatibility with standard silicon technology, low program/erase voltage with high programming speed, and long retention time [3]. Practically, the formation of Si NC layer as floating gate dielectric is the critical process for device performance. Up to now, several technologies have been employed to synthesize the Si NCs, including chemical vapor deposition [4,5], physical vapor deposition like reactive evaporation [6], Si ion implantation into SiO_2 film [7,8], and co-sputtering [9]. However, there seems to be no report about the synthesis of Si NCs by electron-beam co-evaporation (EBCE) and their application to floating gate memory. It is known that electron-beam evaporation, compared to other techniques, has the following advantages: it is fully compatible with standard silicon CMOS process, and it is an efficient way of evaporating a source material and allowing for thin film coatings on substrates. Besides, it can evaporate most materials. Hence, it will be of great potential to synthesize Si NCs by co-evaporating designed Si and SiO_2 source material.

In this paper, Si NCs/SiO_2 hybrid films, synthesized by EBCE of Si and SiO_2, are applied to floating gate dielectric of the metal-oxide-semiconductor (MOS) capacitor devices, and their NVM characteristics are studied. Besides that, the influence of the Si/SiO_2 wt. ratio in source material on the memory characteristics is also experimentally demonstrated and discussed.

2. Experimental details

The EBCE source material is composed of Si and SiO_2. For source material preparation, the Si and SiO_2 solid powders with 45 μm diameter are used. Firstly, the Si and SiO_2 powders are weighted via electronic balance system, respectively. Then, they are well-mixed together as source material, in which the Si/SiO_2 wt. ratio can be adjusted by changing the ingredient of Si as well as SiO_2. At last, the source material is compressed and shaped into tablets before it is loaded onto the evaporation crucible.

For Si NCs/SiO_2 hybrid film fabrication, e-beam evaporation system (EVAP 92, Johnson Ultravac Inc.) is utilized. The chamber is evacuated to ultra-high vacuum up to 1.3×10^{-5} Pa after these tablets are loaded onto the crucible. During the process, the evaporation rate is set up to a value of 0.1 nm s^{-1}. Both the evaporation rate and the film thickness are monitored by the quartz-crystalline oscillator. With careful design, the deposition uniformity is ±0.25% over 3-inch diameter substrate. The silicon-rich silicon oxide (SRSO) layers are synthesized by EBCE at room temperature. Thereafter, the post-deposition annealing (PDA) is carried out to create the Si NCs/SiO_2 hybrid layers with the furnace temperature at 1050 °C for 1.5 h, and the N_2 gas flow of 40 sccm.

For capacitor device fabrication, Fig. 1 shows the schematic cross-sectional structure of MOS capacitor discussed in this paper. First of all, the P type silicon (100) substrates with resistance of 2–3 Ω·cm are chemically cleaned. Then a 5 nm SiO_2 layer is thermally grown on p-

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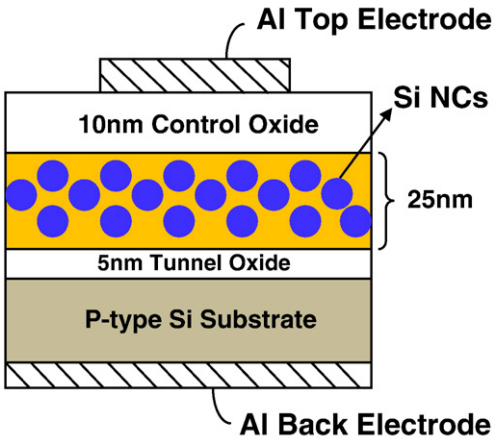

Fig. 1. The schematic view of device structure of MOS capacitor with Si NCs embedded in the gate oxide.

type Si (100) wafers in dry oxygen ambient at 950 °C. After that, to form the SRSO layer, three source materials with different Si/SiO_2 wt. ratios of 22 wt.%, 32 wt.%, and 58 wt.% are evaporated on three separated substrates with the same thickness of 25 nm, named as sample A, B and C respectively. To prepare the Si NCs/SiO_2 hybrid layer, PDA process is performed for all SRSO samples under the condition mentioned above. Then, a 10 nm SiO_2 layer as the control gate dielectric is deposited by low pressure chemical vapor deposition (LPCVD) at 500 °C. The square-shaped Al top-electrodes are defined by standard photolithograph and the lift-off process. Al back-electrode is evaporated on the rear surface of the silicon substrate in all area. Finally, the rapid thermal annealing process is carried out for the alloying under 400 °C for 30 min with N_2 gas flow of 40 sccm. Control sample without Si NCs is simultaneously fabricated under the same process except that 25 nm SiO_2 dielectric layer is deposited by using LPCVD.

The TEM images are obtained by the H9000-NAR (300 kV) high-resolution transmission electron microscopy provided by Hitachi®. Here, for TEM observation, silicon substrate is used. The Raman spectra are measured by Jobin-Yvon T6400 laser micro-Raman spectroscope. In this measurement, quartz substrate is used so as to get rid of the influence from substrate. The charge storage characteristics are investigated using Keithley 4200 semiconductor characterization system combined with 590 *C–V* analyzer at room temperature.

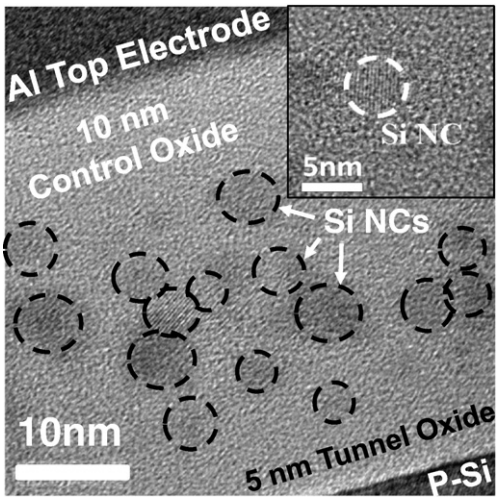

Fig. 2. Cross-sectional TEM image: illustration of the MOS capacitor device structure with inset image of single Si nanocrystal in detail.

3. Results and discussion

The existence of Si NCs embedded in SiO_2 matrix after annealing is clearly observed by cross-sectional transmission electron microscopy (TEM), as shown in Fig. 2. High resolution TEM image of single Si NC, shown in the inset, reveals the distinct lattice fringe patterns, indicating the highly crystalline nature of the Si NCs. According to the TEM image, the silicon nanocrystal density in Si NCs/SiO_2 hybrid layer is 3×10^{11} cm^{-2}. There is a size distribution of Si NCs between 2.5 nm and 7 nm, with the mean diameter of 4.5 nm, which best satisfies the practical application of nanocrystal memory devices [10]. Note that since the growth of Si NCs in SRSO film is a self-assembly process, the size distribution of Si NCs is unavoidable and cannot be controlled precisely.

In order to further characterize the formation of Si NCs after annealing, Raman scattering measurement is performed, as shown in Fig. 3. The as-deposited sample shows the absence of Raman signal. But for the sample annealed, clear and sharp Raman peak centered at 517.7 cm^{-1}, which is denoted as the typical Raman spectrum of Si NCs [11], is observed. According to J. Zi et al. [12] deduced from the original calculation done by I.H. Campbell and P.M. Fauchet [13], the Raman shift of Si NCs can be predicted using the Bond Polarisability Model:

$$\Delta\omega = \omega(d) - \omega_0 = -A(\alpha/L)^{\gamma}, \quad (1)$$

where $\omega(d)$ is the frequency (517.7 cm^{-1}) of the Raman phonon in a nanocrystal with size d, ω_0 (about 520 cm^{-1}) is the frequency of the optical phonon at the zone center for bulk crystal Si, and α is the lattice constant of Si (0.543 nm). The parameters A and γ, used to describe the vibration confinement due to the finite size in a nanocrystal, are 47.41 cm^{-1} and 1.44, respectively. After the calculation according to Eq. (1), d is about 4.4 nm. Here, for calculation, we use the main Raman peak of 517.7 cm^{-1}, where the most intensive Raman signal is observed, indicating that most of the NCs have a diameter of 4.4 nm.

Fig. 4 shows the high-frequency (1 MHz, 300 K) capacitance–voltage (*C–V*) curves of MOS devices embedded with Si NCs under different sweeping voltages. As shown in Fig. 4b, the control sample without Si NCs shows negligible hysteresis, indirectly proving that charging effect only occurs with Si NCs. However, for the sample with Si NCs, a conspicuous counterclockwise hysteresis is observed in Fig. 4a. Here, it should be mentioned that the centre of the hysteresis curve is around −4.5 V, which, in ideal condition, should be near 0 V. This shift may be induced by the excessive immobile positive charges existing in the oxide layer and the work function difference between the Al electrode and silicon [14]. In our work, this flatband shift, may be due to the metal contamination during the evaporation since we use a tungsten crucible. Though it is difficult to be evaporated, the evaporation

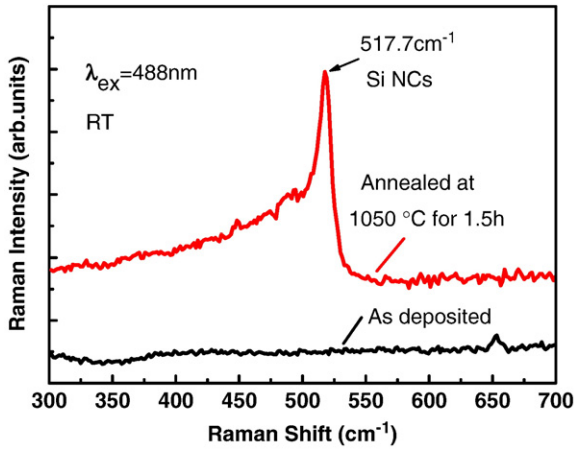

Fig. 3. Raman spectra of the sample with Si NCs and the as-deposited sample, clear and sharp Raman peak from the Si NCs situated at 517.7 cm^{-1}.