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Direct comparison of the electrical properties in metal/oxide/nitride/oxide/silicon and metal/aluminum oxide/nitride/oxide/silicon capacitors with equivalent oxide thicknesses

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ABSTRACT

We examine the electrical properties of metal/oxide/nitride/oxide/silicon (MONOS) capacitors with two different blocking oxides, SiO_2 and Al_2O_3, under the influence of the same electric field. The thickness of the Al_2O_3 layer is set to 150 Å, which is electrically equivalent to a thickness of the SiO_2 layer of 65 Å, in the MONOS structure for this purpose. The capacitor with the Al_2O_3 blocking layer shows a larger *capacitance–voltage* memory window of 8.6 V, lower program voltage of 7 V, faster program/erase speeds of 10 ms/1 μs, lower leakage current of 100 pA and longer data retention than the one with the SiO_2 blocking layer does. These improvements are attributed to the suppression of the carrier transport to the gate electrode afforded by the use of an Al_2O_3 blocking layer physically thicker than the SiO_2 one, as well as the effective charge-trapping by Al_2O_3 at the deep energy levels in the nitride layer.

1. Introduction

Recently, 30-nm-scale charge-trap flash memories based on poly-silicon/oxide/nitride/oxide/silicon (SONOS) structures have been developed as possible replacements for the floating-gate type devices. These SONOS devices have a number of potential advantages such as their simple cell structure, compatibility with the conventional *complementary metal-oxide-semiconductor* process, low voltage operation, two-bit storage capability and radiation hardness [1–3]. However, these devices still suffer from reliability problems, such as a short retention time, which is caused by the reduction in the layer structure as well as de-trapping (or back-tunneling) of the electrons to the gate electrode during the erase operation by Fowler–Nordheim (FN) tunneling [4]. This problem has been reduced by using thicker tunnel oxide and/or blocking oxide layers, but at the expense of a decrease in the program and erase speeds [5,6]. In order to overcome the trade-off problem between the programming speed and data retention in SONOS memories, the use of high-*k* dielectrics such as Al_2O_3, HfO_2 and ZrO_2 as the blocking layers has been intensively studied in the last decade [7–9]. In particular, Al_2O_3 has been widely used as a top dielectric material, since it features a large energy band gap of 8.7 eV, a large conduction band offset of 2.8 eV with respect to silicon and a large dielectric constant of 9 [10].

This approach was quite successful for improving the programming and erasing properties and nowadays many research groups are working with these so-called poly-silicon/aluminum oxide/nitride/oxide/silicon (SANOS) structures for the next-generation charge-trap type flash memory devices. However, almost all of the SANOS structures that have been reported so far take advantages of having higher electric field applied to the tunnel oxide than the top blocking oxide layer by using an Al_2O_3 layer of the same physical thickness, but larger dielectric constant, than the SiO_2 blocking layer [7,11] However, these SANOS structures still suffer from the problem of the increase in the gate leakage currents through the blocking oxide layer and/or the reduction in the charge-trapping efficiencies in the nitride layer, as is the case of conventional SONOS structures, because there is no difference in the physical thicknesses between the Al_2O_3 and SiO_2 blocking oxide layers.

In this work, we prepare two different types of capacitors with either $SiO_2/Si_3N_4/SiO_2$ (ONO) or $Al_2O_3/Si_3N_4/SiO_2$ (ANO) structures of the same electrical thickness in the layer structures, and compare their electrical properties, such as their memory windows, program/erase voltages, program/erase speeds, leakage currents and data retention one-by-one, in order to identify further potential optimizations in the ANO structures.

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2. Experimental details

All of the processes used for making the metal/oxide/nitride/oxide/silicon (MONOS) and metal/aluminum oxide/nitride/oxide/silicon (MANOS) capacitors were identical, except for that of the blocking oxide layer. A tunnel oxide layer was thermally grown on top of silicon at 900 °C and then a nitride layer was deposited using low-pressure chemical vapor deposition (CVD) at 750 °C, by the reaction of dichlorosilane ($SiCl_2H_2$) and ammonia (NH_3) gases. Next, a blocking layer of SiO_2 was deposited for the ONO stack using high temperature oxide CVD, while an Al_2O_3 blocking layer was deposited for the ANO stack using an atomic layer deposition technique. In order to compare the electrical properties of the two samples under the influence of the same electrical field, the electrical thicknesses of the ONO and ANO stacks were calculated so as to take into consideration the physical thicknesses and dielectric constants of Al_2O_3 and SiO_2, such that the ONO stack was 65/60/20 Å thick and the ANO stack was 150/60/20 Å thick. The thicknesses of the ONO and ANO stacks were confirmed using transmission electron microscopy.

Following the film deposition, rapid thermal annealing was conducted for both samples in N_2 gas ambient at 950 °C for 30 s Then, Al metal was deposited on top of the blocking oxide layer using an electron beam evaporator to form the gate electrode. Finally, the current–voltage (*I–V*), capacitance–voltage (*C–V*), and program/erase and data retention characteristics of all of the samples were measured using a *C*-meter (*HP4280A C*-meter), pulse generator (*HP81101A*) and semiconductor parameter analyzer (*HP4156*), respectively.

3. Results and discussion

Fig. 1 shows the *I–V* characteristics measured for the MONOS and MANOS capacitors with the same electrical thickness. The leakage currents are as low as 600 pA for the ONO sample and 100 pA for the ANO sample at a bias voltage of 4 V. The lower leakage current of the ANO sample is thought to result from the use of the thick Al_2O_3 blocking layer, instead of the thin SiO_2 blocking layer in the ONO sample. In the inset of Fig. 1, we can see that charge leakage from the Si substrate to gate electrode can be effectively prohibited by using a thicker Al_2O_3 oxide layer, although the conduction band offset between the Al_2O_3 and Si_3N_4 (~2.8 eV) is smaller than that between the SiO_2 and Si_3N_4 (~3.5 eV) [12,13]. The inset figure shows the energy band diagram when the same electric fields are applied to both the ONO and ANO structures. Basically, the magnitude of electrical fields that can be applied to each layer of the two samples should be equivalent because we used electrically equivalent oxide thicknesses for both samples, according to the equation in Ref. [14]. However, the

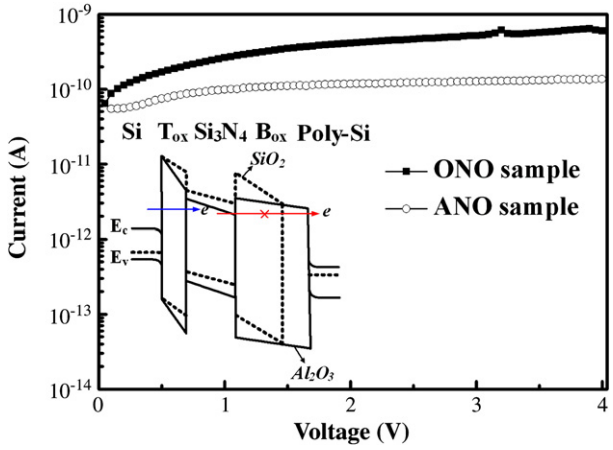

Fig. 1. Leakage currents measured for both the MONOS and MANOS capacitors with the same electrical thickness.

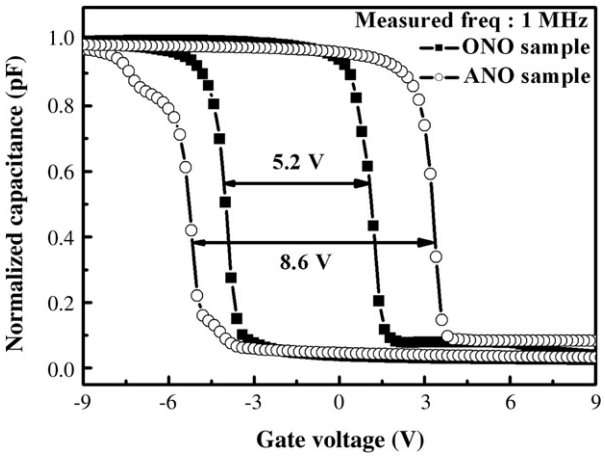

Fig. 2. *C–V* hysteresis measured for both the MONOS and MANOS capacitors with the same electrical thickness.

electric field distributions across the layers can be different for both samples depending on the film qualities (i.e., interface traps between Al_2O_3 and Si_3N_4 or bulk traps in Al_2O_3 blocking layers [15] and/or gate bias conditions [16]), which can lead to the difference in the characteristics of the two difference structures.

Fig. 2 shows the *C–V* memory window versus gate voltages for the MONOS and MANOS capacitors with the same electrical thickness. The gate biases were varied from −9 to 9 V at a frequency of 1 MHz during the *C–V* sweep. In the normalized *C–V* hysteresis curve, the *C–V* memory window of the ANO sample was found to be as large as 8.6 V, whereas it was only 5.2 V for the ONO sample. This result indicates that more charges are trapped in the ANO structure than in the ONO one, although the thickness of the Si_3N_4 trapping layer (60 Å) is the same in both cases. In general, electrons are initially injected from the channel through the tunneling oxide during the application of a positive bias for programming and, then, the injected electrons can be captured by the traps in the nitride layer. However, in the case of the ONO structures with a 65 Å thick blocking oxide layer, electrons captured in the traps can be readily de-trapped and move to the blocking oxide under the influence of the applied field. Some of these de-trapped electrons can be injected even into the gate by a large electrical field, eventually lowering the charge-trapping efficiency. On the other hand, for the ANO structures with a 150 Å thick blocking oxide layer, such electron de-trapping is rarely observed under the same bias conditions, because only a few electrons can pass through the thick blocking oxide layer once the electrons are trapped in the nitride layer, thus increasing the charge-trapping efficiency.

In order to compare the program efficiency between the two samples, we measured the flat band voltage (V_{FB}) shift as a function of the program voltage during a program time of 1 s, as shown in Fig. 3. Here, V_{FB} is defined as the applied gate voltage at which the normalized capacitance is 0.8 pF [17]. The V_{FB} shift of the ANO sample was observed to be greater than that of the ONO sample at program voltages below 9 V, whereas there was little difference between them at program voltages above 9 V. For instance, a V_{FB} shift of 2 V, which is large enough for program operation, was observed at 7 V for the ANO structure, while the same shift was observed at 9 V for the ONO structure. Although 7 V is not good enough for low-voltage programming, when considering the previous values reported in the literature [1], it is interesting to find that the operating voltages for programming in the ANO structure are always lower than those in the ONO one. It is expected that an additional reduction in the programming voltage can be achieved through the optimization of the layer structure.

In addition, we monitored the *C–V* curves of the ONO and ANO samples for various program times at a fixed gate voltage ($V_g = 9$ V),