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Impact of line width roughness on the matching performances of next-generation devices

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Abstract

It is now widely accepted that line width roughness (LWR) reduces transistor performances and is a critical factor, along side gate leakage and short-channel effects, for device scaling at the 45 nm technology node and beyond. As new process modules and device architecture options are emerging, we report on a methodology that has been developed to study the impact of line width and LWR uncertainties at the device level. By investigating the matching performances of both planar CMOS and FinFETs, we evaluate the sensitivity to roughness of important electrical parameters like the off-current or the threshold voltage.

Keywords: LER; Matching; FinFET

1. Introduction

Scaling of CMOS technology over the past decades has pushed a number of variability mechanisms to the point where they have become significant factors in circuit design. It has promoted variability to a first-order key limitation to continuous technology scaling.

Parameter variations may be deconvolved into random and systematic components: those that involve the chip mean, those that vary within the chip but have local or chip-to-chip correlation, and those that vary randomly from device to device. These intrinsic variations are caused by atomic-level differences that occur even though the devices are located close together and have identical layout geometry and environment. These stochastic differences appear in: dopant profiles, film thickness variation, and LWR. All these differences give rise to fluctuations in the electrical parameters of a device, with an amplitude strongly dependent on the process options used in transistor fabrication.

When defining a process for a new technology node and for a target application (high-performance, low-power), it becomes mandatory to find a good balance between the intrinsic Figures of Merit of a device like the threshold voltage, subthreshold behavior or leakage properties, and their sensitivity to sources of random fluctuations.

In this paper, we use matching performances of advanced CMOS technologies as a means of probing the impact of line width and LWR uncertainties at the device level. Section 2 first describes frameworks that have been developed for the characterization of line-edge roughness. In Section 3, we evaluate the sensitivity to roughness of important electrical parameters like the off-current or the threshold voltage for both planar CMOS and multiple-gate devices known as FinFETs. Recent works and future requirements related to metrology of 3D devices are presented in Section 4. Finally, conclusions are outlined in Section 5.

2. Characterization of line-edge roughness

2.1. Spatial frequency analysis

LWR is studied often from a lithography perspective during patterning. Many factors contribute to LWR including: resist composition [1], aerial image contrast [1–4], development [1,4] and process conditions [3–5]. The roughness is usually measured with top down critical dimension scanning electron microscope (CD-SEM) or using off-line analysis for corresponding SEM pictures. The LWR is usually characterized by the 3σ value. Table 1 indicates the some parameters for

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Table 1
ITRS requirements for variability at the lithography level

Year of production	2010	2013	2016
DRAM half pitch [nm]	45	32	22
Printed gate length [nm]	25	18	13
Physical gate length [nm]	18	13	9
Line width roughness 3σ [nm]	1.4	1.0	0.7
Gate length uniformity 3σ [nm]	1.6	1.2	0.8

future technology nodes. However, previous work showed that it is not sufficient to measure only the 3σ variation [5–7].

A more complete description of the LWR can be obtained by measuring the full spatial frequency-dependence of the roughness. All this makes the comparison and quantification of line-edge roughness more difficult. Besides σ, the spatial frequency components can be resolved using a power spectral density (PSD) function, height–height correlation function or assuming a first-order autoregressive process. The spatial frequency-dependence can be described by two additional parameters that quantify the spatial aspects of LWR: the roughness exponent (α) and the correlation length (ζ). The roughness exponent is associated with the fractal dimension $D(\alpha=2-D)$ [8] and its physical meaning is that it gives the relative contribution of high frequency fluctuations to LWR. The correlation length (ζ) represents the cut-off frequency in Fourier space. The standard deviation of edge points (σ) is a direct measure of the edge roughness itself. Large values of α indicate less high frequency fluctuations. On the other hand, the correlation length denotes the distance after which the edge points can be considered uncorrelated.

2.2. Impact of advanced lithography options

The lithography options for (sub-) 45 nm technology nodes are not known yet. There are two main competitors: 193 nm immersion lithography and Extreme Ultra Violet (EUV) lithography, both with their own characteristic impact toward the LWR performance of the resist.

With respect to immersion lithography, the tools are expected to show the same stability and control as the equivalent dry systems. Therefore CDU, focus and overlay control are being evaluated. New aspects arise with respect to photo resist processing and defectivity due to the interaction with water. Photo resists developed for dry 193 nm lithography showed significant leaching of PAG, acid and quencher, as well as water uptake when immersed in water [9]. Resists need to be optimized for this, and in the mean time immersion top coats are introduced to overcome this leaching [10], and dedicated resists are being optimized for use without a top coat. The leaching of resist components or the penetration of water in the resist layer has an impact on the CD control [11]. It is also found that the LWR performance of the resist can perform differently.

For EUV lithography, the available illumination power is limited, leading to statistical (shot noise) variations. The statistics of photon arrival gives rise to local dose variations, which translate to local variations in the size of written features or LWR [12]. In addition, owing to the extremely short wavelength and reflective nature of EUV optics, scattering (flare), is a significant concern. Roughness in the range of 1 μm–1 mm frequency range causes small-angle scattering of light off the mirror surfaces. This scattering causes a reduction in the contrast of images because it scatters light from bright regions of the image plane onto regions intended to be dark. This scattering is often called flare. Because the effects of scatter scales as $1/\lambda^2$, the deleterious effects of flare are becoming more evident for EUV lithography ($\lambda=13.5$ nm). Fig. 1 shows the degradation of LWR with increasing flare levels (0%–40%) for an experimental EUVL resist. The LWR increases for this resist from $3\sigma=7$ nm to $3\sigma=11$ nm for 0% to 20% flare levels, respectively.

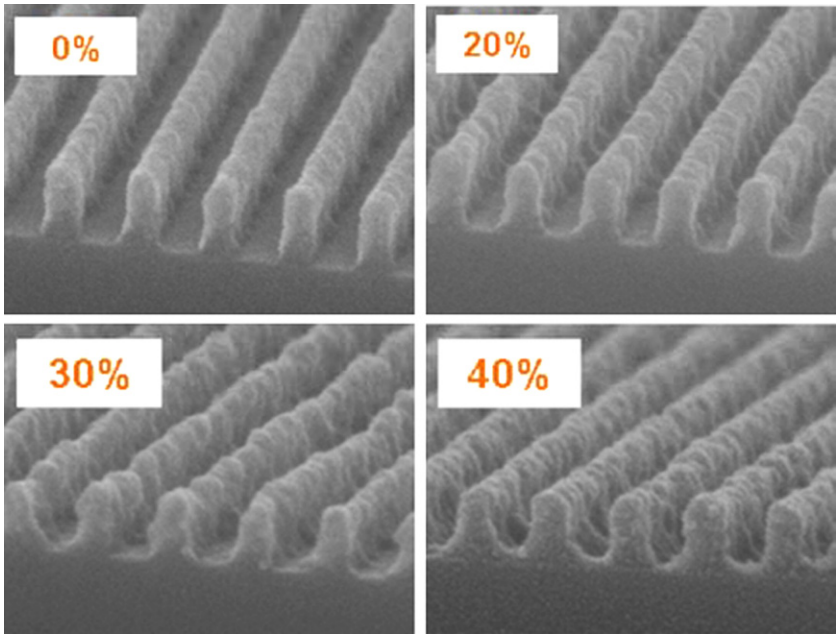

Fig. 1. Top-down CD-SEM pictures showing the impact of increased flare on the roughness of 50 nm lines and spaces.