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Analysis of ITO thin layers and interfaces in heterojunction solar cells structures by AFM, SCM and SSRM methods

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Abstract

Atomic force microscopy (AFM), scanning capacitance microscopy (SCM) and scanning spreading resistance microscopy (SSRM) were used for the analysis of the morphology and electrical properties of heterojunction (HJ) solar cell structures made of Indium Tin Oxides (ITO) layers deposited on p-type polished Si substrates with a buffer layer of n-type hydrogenated amorphous Si (a-Si:H). By means of AFM measurements it is shown that the a-Si:H layer can be deposited on a Si substrate quite homogeneously with a roughness of only a few nanometers. In contrast, the morphology of the ITO layers depends on the deposition temperature and can be varied during the HJ solar cell processing. Cross section analysis of the HJ structures by SCM shows penetration of n-type carriers into the (p)Si bulk substrate and the formation of the resulting n–p electrical junction depends strongly on the ITO deposition temperature and the presence of the (n)a-Si:H layer. Complementary cross section SSRM measurements show only a highly n-type doped region confined to the ITO layer. Finally it is concluded that the properties of the HJ solar cell structures depend dramatically on the properties of the ITO layers and can be modified by variation of the ITO deposition temperature.
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Keywords: AFM; SCM; SSRM; ITO; Silicon; Heterojunction solar cells

1. Introduction

The low-temperature approach for processing of Si-based heterojunction (HJ) solar cells is an attractive strategy, which can be regarded as an alternative for the conventional high-temperature technology. A successful realization of this strategy was demonstrated by SANYO for n-type Si substrates [1], while for p-type Si substrates, in spite of the worldwide activity in this field, the problem is not solved [2]. It is well established long time ago that heterojunction solar cells offer potential design advantages over homojunctions, but it has also become apparent that heterojunctions introduce a whole set of problems at the metallurgical junction [3]. In the case of HJ structures consisting of Indium Tin Oxides (ITO) layers deposited on p-type polished Si substrates ((p)Si) with a buffer layer of n-type hydrogenated amorphous Si layer ((n)a-Si:H) these problems occur at the interfaces between the very thin ITO (~80 nm) [4] and (n)a-Si:H (~5–30 nm) [4,5] layers as well as at the a-Si:H/Si interface [5–9]. Therefore, an analysis of the individual layers and interfaces of these structures has to be done by means of methods with a high spatial resolution, such as atomic force microscopy (AFM), scanning capacitance microscopy (SCM) and scanning spreading resistance microscopy (SSRM), which provide a possibility to investigate features on a nano-scale. It is necessary to note that SCM and SSRM have proven to be a powerful techniques for carrier density profiling in semiconductor materials and devices [10,11]. Advantages with those scanning probing methods (SPM) include high sensitivity to doping variation and high lateral resolution [12,13].

The goal of this work is to investigate the behaviour of the individual (n)a-Si:H and ITO layers and their interfaces in ITO/(n)a-Si:H/(p)Si structures while forming HJ's. For a comparison, also ITO/(p)Si and (n)a-Si:H/(p)Si layers have been investigated. Moreover a comparative analysis of HJ structures formed by ITO layers deposited at different temperatures is performed to clarify the role of the ITO deposition temperature.

2. Experimental

ITO/(n)a-Si:H/(p)Si structures were performed by deposition of (n)a-Si:H and then ITO layers on p-type polished Cz Si

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substrates with a resistivity of 1–3 Ω cm and orientation (100). The n-type 5 nm thick a-Si:H layers were deposited using a conventional plasma-enhanced chemical vapor deposition (PECVD) system with the following parameters: 24 sccm flow rate for SiH_4 and 12 sccm for PH_3 (3% PH_3 diluted in SiH_4), 39.9 Pa (300 mTorr) deposition pressure, 13.56 MHz frequency, 4.3 W power, 230 °C deposition temperature. Such parameters were used since it has been shown earlier that (n)a-Si:H layers deposited under such conditions yield HJ solar cells with efficiencies around and even above the 15% [9,14]. Immediately after the (n)a-Si:H deposition, ITO layers were deposited by magnetron sputtering at room temperature (RT) and at 230 °C to a thickness of 70–80 nm. An ITO sintered target, with In_2O_3 and SnO_2 in a weight proportion of 9 : 1, was used. The base pressure in the sputter system was about 1.33 mPa (10^{-5} Torr). The total pressure of sputtering gas mixture was adjusted to 0.399 Pa (3 mTorr) during the film preparation. The argon flow rate and the DC plasma power were kept constant at 38 sccm and 100 W, respectively, at both deposition temperatures.

The AFM, SCM and SSRM measurements were performed using Digital Instrument's Nanoscope Dim 3100 microscope equipped with spreading resistance and capacitance measurement electronics. The AFM measurements were performed in tapping mode using commercial silicon tips MikroMasch NSC35/AlBS with a typical tip curvature radius of less than 10 nm. The following parameters for the analysis of the AFM measurements were used: (i) the Root Mean Square (RMS) Roughness (R_q), which gives the root mean square average of height deviations taken from the mean data plane within a given area; (ii) the Mean Roughness (R_a), which represents the arithmetic average of the absolute values of the surface height deviations measured from the mean plane; (iii) the difference in height between the highest and lowest points on the surface relative to the mean plane (h_{max}); (iv) the average differences of heights (h_{aver}) [15]. The SCM and SSRM measurements were performed on the cross sections of the HJ structures. The cross sections were obtained by manually cleaving the samples. Then the structure was embedded into the conductive silver paste in order to create back electrical contact. For both the electrical SPM measurements the topography of the cross section was measured simultaneously by AFM in order to exclude any topography induced features. The SCM measurements were performed using commercial conductive Ti–Pt coated silicon tips MikroMasch NSC18 with a microscopic tip radius less than 40 nm. For the SCM measurements the tip and the sample form a metal-insulator–semiconductor capacitor including a native insulating layer formed on top of the cross section. The SCM measurements were performed in so-called dC/dV mode with a fixed ac modulation voltage frequency of 90 kHz applied to the SPM probe. For constant amplitude of the ac voltage (dV) the magnitude of capacitance variation (dC) is in general a nonlinear decreasing function of the carrier density [13]. It is necessary to note that dC/dV amplitude signal is zero for regions with both, very high or very low carrier densities or for regions with the equal amount of n- and p-type carriers. In addition, the SCM phase is normally sensitive to the carrier type. The phase lock-in was chosen in such a way that positive (around +90°) and negative (around −90°) values of the measured SCM phase indicate p- and n-type carriers, respectively. An additional dc bias applied to the SPM probe acts as a static electrical field perpendicular to the investigated structure and provides a possibility to deplete or enhance the carrier density beneath the probe depending on the polarity of applied dc bias. The SSRM measurements were performed using commercial conductive B-doped diamond coated silicon tips NanoSensors CDT/NCHR with a microscopic tip radius of 10 nm (on nanoroughness). A dc bias was applied to the tip and the current flowing through the sample was measured by a logarithmic current amplifier. In SSRM the measured current is sensitive to the bias amplitude and polarity due to the formation of a Schottky-like contact. Therefore, for reliable measurements an appropriate tip pressure and dc bias amplitude were applied. The acquired SSRM data was converted by standard procedure to the spreading resistance, which in general can be directly related to the material resistivity and carrier density [16]. In order to improve signal to noise ratio only averaged lines derived from the SCM and SSRM images data were used for the investigations presented in this work.

3. Results and discussions

Fig. 1 shows the surface morphology of a 5 nm thick (n)a-Si:H layer deposited on a polished p-type Si substrate. From Fig. 1 it can be concluded that in spite of the fact that (n)a-Si:H layer is very thin the PECVD process gives a rather homogeneous layer with some local peculiarities, which may be attributed to nano-Si particle formation during the (n)a-Si:H deposition (for corresponding AFM parameters see Fig. 1 capture). It is interesting to note that the size of the nano-Si particles is comparable with the thickness of the (n)a-Si:H layer.

Fig. 2 displays the surface morphology of ITO layers deposited on (n)a-Si:H/(p)Si substrates at RT and 230 °C. For a comparison ITO layers were deposited directly on (p)Si

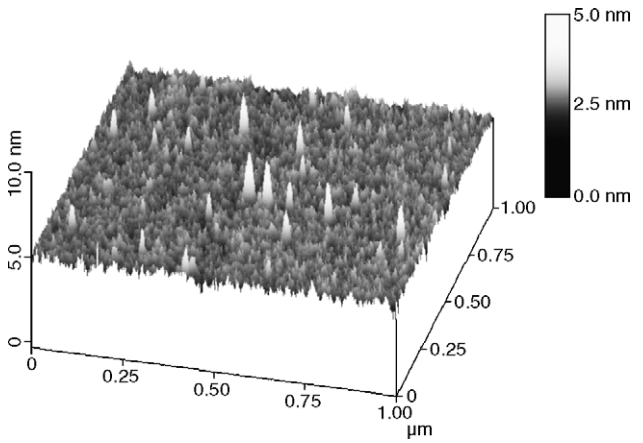

Fig. 1. AFM 3D image of (n)a-Si:H layer deposited at 230 °C on a p-type polished Si substrate (R_q=0.22 nm, R_a=0.16 nm, h_{max}=3.9 nm, h_{aver}=2.8 nm).

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