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Interface properties of a-Si:H/c-Si heterojunction solar cells from admittance spectroscopy

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Abstract

The capabilities of admittance spectroscopy, in particular the dependences of the admittance upon frequency, temperature and applied bias, for the investigation of a-Si:H/c-Si heterojunctions are presented. Experimental results and results from a numerical modelling are described for n-type a-Si:H/p-type c-Si heterojunctions. These results compare very well and show that the admittance technique is sensitive to parameters of the a-Si:H/c-Si interface quality. The influence of different interface parameters, such as absolute value of defect density, hole and electron capture cross-sections is studied by the simulation. This simulation tool enables a detailed analysis of experimental results. In particular, it allows us to precise whether the capacitance signal is related to exchanges between interface states and electrons from the a-Si:H or (and) holes from the c-Si. The application of the admittance technique for a rapid a-Si:H/c-Si interface characterisation is discussed.

Keywords: Heterojunction; Solar cells; Capacitance technique

1. Introduction

The characterization methods of interface properties are very important tools for the study and fabrication of any semiconductor heterojunction device. In particular, heterojunctions between hydrogenated amorphous silicon (a-Si:H) and crystalline silicon (c-Si) are of great interest for photovoltaic application due to the high solar cell efficiencies achieved so far (up to 21%), and the possibility of complete fabrication at low temperature process [1]. The properties of the a-Si:H/c-Si interface are one of the critical issues for the photovoltaic application because the recombination at interface states may significantly decrease the solar cell efficiency. Thus, efficient methods of interface characterisation are needed to study interface properties and to optimise the fabrication process.

It is known that the frequency and temperature dependence of the junction admittance is very sensitive to exchanges with trap levels and its variations with applied dc bias are strongly dependent on interface properties [2,3]. Recently, admittance spectroscopy has been successfully applied to study the interface properties of a-Si:H/c-Si heterostructures [4–7]. It was shown that, generally, in the experimental temperature dependence of the capacitance ($C-T$) two steps may be observed that are shifted to higher temperature with increasing the measuring frequency. The first step occurring in the low temperature range (100 K–200 K), accompanied by a corresponding bump in $G-T$ curves, is related to the transport and response of gap states in the a-Si:H layer [5,7]. The position of this step and frequency spreading are determined by the position of the Fermi level and capture cross-section of the states in a-Si:H, and the absolute value of the capacitance step is determined by the difference between layer thickness and depletion length in the a-Si:H layer. The detailed analysis of the influence of different parameters of the a-Si:H layer on this step has been reported in Ref. [7]. The second step occurring at higher temperature (>200 K) was explained by the response of the interface states. We here focus on the analysis of the latter

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Table 1
Main parameters of heterojunction layers used in the simulations

Parameter	(n)a-Si:H	Interface layer	(p)c-Si	(p+)c-Si
Band gap, eV	1.8	1.12	1.12	1.12
Doping density, cm^{-3}	10^{19}	7×10^{14}	7×10^{14}	5×10^{18}
Fermi level (to the nearest band), eV	0.2	0.248	0.248	0.015
Electron affinity, eV	3.85	4.05	4.05	4.05
Thickness, cm	10^{-6}	10^{-7}	0.3	10^{-4}

capacitance feature using both the results of simulations of admittance spectra and the results of experimental measurements for (n)a-Si:H/(p)c-Si heterojunctions.

2. Experiment and simulation details

The ITO/(n)a-Si:H/(p)c-Si/(p+)c-Si heterojunction solar cells were fabricated on p-type c-Si substrates (<100> oriented, thickness of 300 μm, resistivity of 14–22 Ω cm) with Al back surface field contacts. After a HF treatment of c-Si surface a very thin (3 nm) intrinsic pm-Si:H layer was deposited for better passivation of the surface [8] and a thin n-type a-Si:H (12 nm) layer was deposited as the emitter. Both pm-Si:H and a-Si:H layers were deposited by PECVD at an RF frequency of 13.56 MHz under various conditions [9]. Then a 90 nm thick TCO anti-reflection layer was deposited by DC-magnetron sputtering. The structures were completed by screen printing of Ag grid.

The admittance measurements as a function of temperature, frequency and bias ($C-T-\omega$, $G-T-\omega$, $C-V-\omega$) were performed in a liquid nitrogen cryostat in the temperature range 90–350 K using a HP4284A impedance meter at frequencies in the range 20 Hz–1 MHz.

The modelling of the heterostructure admittance and its dependence on temperature, frequency and bias was made using a numerical PC program, AFORS-HET, developed at Hahn-Meitner-Institut in Berlin (HMI) [10]. We considered a single heterojunction between n-type a-Si:H and p-type c-Si, with a rear p+ c-Si layer corresponding to the BSF contact. The front and back contacts were assumed to be ohmic. The material parameters used in the numerical calculations for the c-Si and a-Si:H layers are given in Table 1. The distribution of the density of states (DOS) in a-Si:H were taken according to Ref. [11] as consisting of two exponential band tails with characteristic energies, kT_c, and kT_v, of 0.03 and 0.05 eV for the conduction and valence band, respectively, and with a pre-exponential factor of 4×10^{21} cm^{-3} eV^{-1}, and two Gaussian deep defect distributions of donor and acceptor nature being located at 0.6 and 0.7 eV above the valence band maximum, respectively, with a maximum value of 2.4×10^{19} cm^{-3} eV^{-1} and a standard deviation of 0.15 eV. The value of the conduction band offset was chosen equal to 0.2 eV. The interface was described by introducing an interface layer with a thickness of 1 nm between c-Si and a-Si:H. The defect distribution in this interface layer was assumed to be constant within the bandgap, assuming donor/acceptor-like defects in the lower/upper part of the bandgap. In the following D_{it} (in cm^{-2} eV^{-1}) will denote the interface defect density, which is determined as the product $d_{int}\times g_{it}$, where d_{int} is the thickness of the interface layer (1 nm) and g_{it} (in cm^{-3} eV^{-1}) is the DOS in this layer. In order to study the influence of interface defects we varied D_{it} and the electron and hole capture cross-sections (σ_n and σ_p, respectively), while the parameters of the c-Si and a-Si:H layers were kept constant.

3. Experimental results

The admittance measurements performed on a large number (more than thirty) of (n)a-Si:H/(p)c-Si heterojunctions obtained with different interface treatment and under different deposition conditions allows us to divide the samples into three major groups. In this paper each group will be represented by one characteristic sample (samples #1, #2 and #3).

The experimental $C-T-\omega$ curves measured for these characteristic samples are presented in Fig. 1. A small monotonic increase of the capacitance with temperature observed for all samples is due to the statistical shift of the Fermi level in both c-Si and a-Si:H, reducing the built-in potential and thus the width of the space charge region with increasing temperature. The sample #1 with a-Si:H layer thickness of 80 nm exhibits a small step in capacitance at low temperature (90–150 K) caused by the activation of transport in a-Si:H. The presence of the step in sample #1 and its absence for samples #2 and #3 (with only 12 nm thick a-Si:H layers) is in good agreement with the simulation made using a-Si:H parameters described below [5,7].

The main difference between samples comes from the presence and form of the step in capacitance curves at higher temperatures (HT step). The sample #1 exhibits a significant capacitance step at a temperature above 250 K, the sample #2 has a much smaller step at slightly lower temperature (200 K), while sample #3 does not have any visible step at all. The observed capacitance HT step is shifted to higher temperatures with increasing frequencies. This shift in the temperature

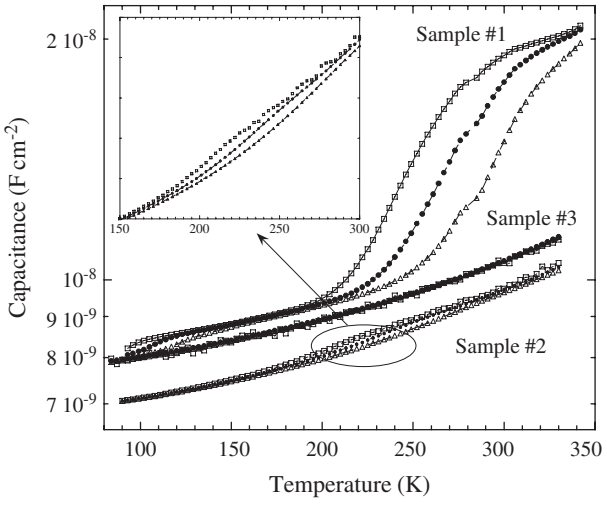

Fig. 1. Experimental $C-T-\omega$ curves for the three characteristic samples measured at zero bias and at the frequencies of 100 Hz (□), 1 kHz (●) and 10 kHz (Δ).