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Surface energy and adhesion energy of solution-based patterning in organic thin film transistors

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Abstract

This study elucidates the patterning of pentacene by adjusting its surface energy. The surface energy was modified by self-assembled monolayer treatment and exposure to ultra-violet (UV) light through a quartz-glass mask. Then, following pentacene deposition, dipping in water was used to remove pentacene from the UV-exposed area. The adhesion energy and the intrusion energy were analyzed to determine the mechanism of this patterning process. The variation of the intrusion energy with the surface energy was found to be the main issue in pentacene patterning. The characteristics of pentacene-organic thin film transistors were also measured to confirm the proposed method.

Keywords: Pentacene; Surface energy; SAM

1. Introduction

The pentacene-based organic thin film transistor (OTFT) has received much attention because it is fabricated at low temperatures on plastic substrates at low cost [1–3]. Carrier transport in pentacene-based OTFT is generally dominated by the characteristics of the interface between the pentacene film and the gate dielectric [4,5]. Numerous studies of the self-assembly monolayer (SAM) have been performed to modify effectively the gate dielectric surface to improve carrier mobility [6,7]. The SAM layer changed the gate dielectric surface from hydrophilic to hydrophobic, enabling the pentacene molecules to align vertically to form the π-orbital. Additionally, given suitable process design, the difference between the hydrophilic and hydrophobic properties is important in the patterning of an organic film [7–9].

Recently, Masahiko Ando et al. demonstrated a simple method for controlling surface polarity (hydrophilic or hydrophobic) using an SAM layer and exposure to ultra-violet (UV) light to pattern the pentacene film [10]. However, the details of the variation of the surface energy have not been discussed. The method left the unwanted high-resistivity pentacene film around the pentacene channel; this may cause cross-talk and the flow of leakage current in OTFT array. Furthermore, the exposure of the backside to UV light depends on a highly transmitting substrate, such as quartz-glass. Such a substrate limits the range of applications since several plastic substrates do not exhibit high transmissivity. This study develops a top-exposure method that can be easily combined with conventional lithography using a quartz mask. The film was dipped into de-ionized (D.I.) water to remove the unwanted pentacene film and prevent crosstalk and the flow of leakage current. The interfacial binding energy and the intrusion energy were analyzed to demonstrate that the dipping was a lift-off process and that the patterning complete was governed by the intrusion among pentacene, the substrate (hydrophilic or hydrophobic) and the D.I. water.

2. Experiments

In the patterning of the pentacene film, an attempt was made to control the surface polarity by exposure to UV light (wavelength: 175–285 nm, power: 40 mW, dose: 0.043 mW/

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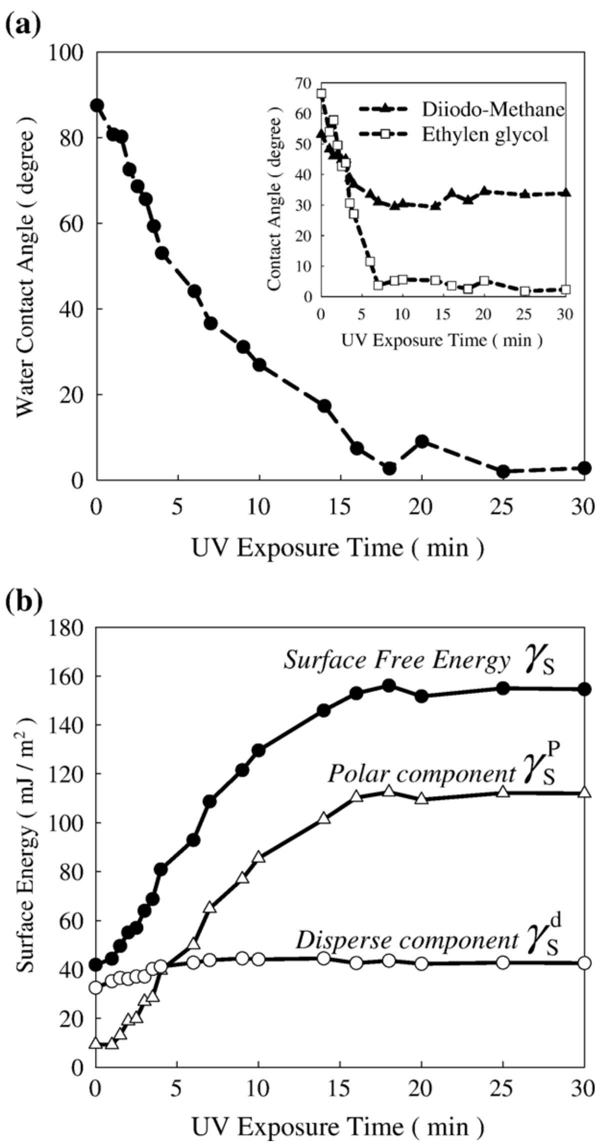

Fig. 1. Effect of exposure time to UV light on (a) the surface contact angle and (b) the polar and disperse components of the surface free energy following ODMS treatment.

cm^2). First, the silicon oxide was cleaned by acetone, isopropanol and acetone solution in that order. Then, the sample was dipped in the dissolved liquid ODMS to make the surface of the silicon oxide hydrophobic. The concentration of ODMS was 10 mM. Then, the surfaces were partially exposed to UV light for time varying from 0 to 30 min. As displayed in Fig. 1, the contact angle and the surface free energy were controlled by the duration of exposure to UV light. The contact angle was obtained by the Contact Angle System of KRÛSS for universal surface testing (model GH-100). Three standard liquids (D.I. water, diiodo-methane and ethylene glycol) were applied to measure contact angles and thus extract the surface free energy of the dielectric. Then, the surface free energy was calculated using the Fowkes and Young approximation [11,12].

To clearly compare the device characteristics, the device fabricating process was split into two parts. In the first part, the pentacene active region was defined by shadow mask. It was deposited by thermal evaporation onto regions that had undergone ODMS treatment (Sample A) and onto regions that had undergone ODMS treatment followed by 30 min of exposure to UV (Sample B). The scale of shadow mask ranged from 300 μm to 700 μm and the scale of UV exposure mask was several centimeters. The thickness of the pentacene film was around 100 nm and the deposition rate was ~ 0.5 Å/s. 100 nm-thick Au pads were deposited through a shadow mask as source/drain contacts. Then, all of the samples were dipped in D.I. water and both the pentacene film and the source/drain contact in Sample B were lifted-off. Sample A′ refers to sample A after dipping in D.I. water to check the functionality of the transistors.

In the second part, the scale of the UV exposure mask ranged from 300 μm to 700 μm to define the pentacene active region without using the shadow mask. Sample A″ was the devices fabricated by the proposed lift-off method. The process conditions of Sample A″ were the same as those of Sample A′, except that the pentacene patterning methods was different. The width and length of the device channel were defined as 600 μm and 200 μm. An OTFT was fabricated using a conventional

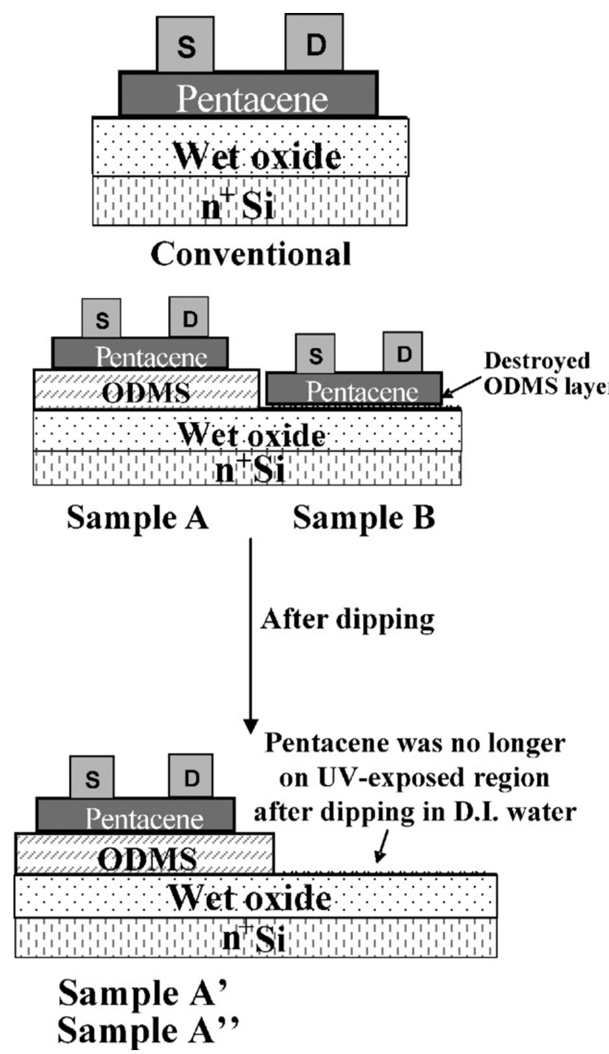

Fig. 2. The fabricated OTFT under various conditions.