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InP-based IC technologies

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Abstract

The research and development of InP-based devices and integrated circuits (ICs) are driven by applications in broadband optical-fiber communications systems and microwave and millimeter-wave wireless systems. This paper describes recent progress on our InP-based device and IC technologies for 40-Gbit/s optical fiber communications and 10-Gbit/s class millimeter-wave wireless links. Device performance requirements for future 100-Gbit/s class ICs are then discussed along with our device technology roadmap. We also describe our latest 100-Gbit/s class optical fiber communication IC results.
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Keywords: Indium phosphide; Electronic devices; Semiconductors

1. Introduction

High-speed IC technology is the key to the development of cost-effective high-speed optical communications systems and microwave/millimeter-wave wireless systems. In optical fiber telecommunications, 10-Gbit/s systems now have a large commercial market, and 40-Gbit/s SONET/SDH [1] and OTN [2] frame formats have been standardized. Work on the technological aspects of 40-Gbit/s ICs has reached the stage where cost-effective commercial products are being developed. The competing technologies in this area are InP, GaAs and SiGe. The interface speeds of telecommunications and data communications systems like the Ethernet have increased by a factor of 4 and 10, respectively. The timescales for the increase in interface speeds are around every 5 years for telecommunications and around every 3 years for data communications, respectively. This means that, if current trends continue, the next-generation interface speeds will be 160 Gbit/s for the former and 100 Gbit/s for the latter.

Bit-rate increase in the data communications is also creating new demands for high-speed wireless local area networks (LANs) and personal area networks. The various version of wireless LANs currently in use feature bit rates of around 20–50 Mbit/s. However, new techniques, such as ultra-wide band and millimeter-band wireless 1394, are expected to enable data rates of 1 Gbit/s in the near future. In addition, 10-Gbit/s wireless links are also expected to be used for temporary broadband networks in natural-disaster recovery efforts, at event halls and venues, and in remote broadcast [3].

InP-based ICs are promising candidates for these high-speed communication systems because of their excellent high-frequency response and high-breakdown voltage. This paper describes recent progress on our InP-based device and IC technologies for 40-Gbit/s optical fiber communications and 10-Gbit/s class millimeter-wave wireless links. Device performance requirements for future 100-Gbit/s class ICs are then discussed along with our device technology roadmap. We also describe our latest 100-Gbit/s class optical fiber communication IC results.

2. 40-Gbit/s InP-based optical communication ICs

2.1. Optical transmission front-end ICs

Fig. 1 shows an example of the basic transmitter and receiver configurations. In the transmitter, parallel low-bit-rate signals are multiplexed by the mulitiplexer (MUX) and then reshaped

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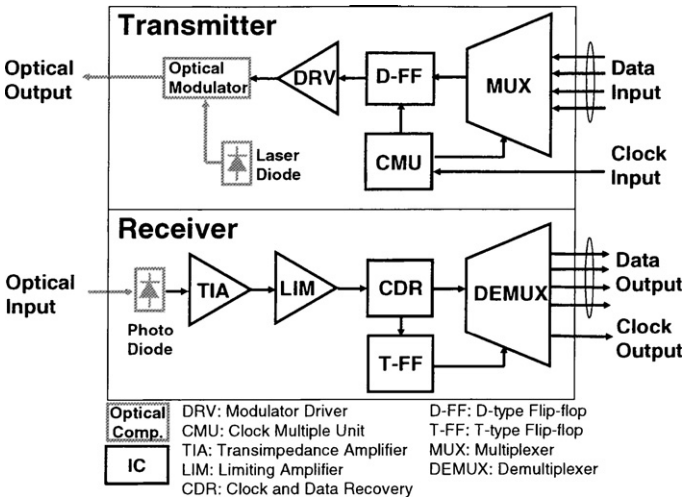

Fig. 1. Basic transmitter and receiver configurations.

by a D-type flip-flop (D-FF), using the full-rate clock signal from the clock multiplier unit (CMU). The modulator driver (DRV) amplifies the output of the D-FF and drives the optical modulator. In the receiver, a photodiode converts the optical signal into an electrical one, which is then amplified by a transimpedance amplifier (TIA) and a limiting-amplifier (LIM). The clock and data recovery circuit (CDR) regenerates and retimes the received electrical signal, and the demultiplexer (DEMUX) then recovers the original parallel low-bit-rate signals.

Analog ICs in the receiver like the TIA and LIM are generally required for 70% bandwidth of the data rate with flat phase characteristics [4], while the DRV in the transmitter requires both broadband characteristics and high saturation output power. As for digital ICs, the D-FF and CDR are critical components that limit the system speed, because they operate at the data rate with a full-rate clock signal that is the same as the data rate. Fig. 1 shows an example of a full-rate system. A system in which the D-FF is eliminated and CDR operates with the half the data-rate clock (half-rate system) mitigates the speed requirement for the electrical components. The full-rate system is, however, superior to the half-rate system in the system margin and robustness.

Table 1
Performance of 40-Gbit/s InP HEMT ICs

Circuit	Operating speed	Output (V_{pp})	Power (W)
TIA	Z_t=48.2 dBΩ, $f_{3\ dB}$=43 GHz	0.46	0.35
Limiting Amp.	Gain=25.4 dB, $f_{3\ dB}$=32 GHz, DC—50 Gbit/s, sens.: 27 mV at 43 G	1.3	0.6
Distributors	Data: DC—50 Gbit/s	1.1	1.6
	Clock: 2–47 GHz	1.0	0.5
CDR	43 Gbit/s, sens.: 175 mV	1.2	2.8
D-FF	20–50 Gbit/s, P.M.: 101° at 50 G	0.9	1.7
T-FF	8–50 GHz	0.8	1.1
4-bit MUX	7–50 Gbit/s, P.M.: 170° for 12.5-G input	1.0	1.7
4-bit DEMUX	4–50 Gbit/s, sens.: 235 mV, P.M.: 234° at 50 G	0.53	1.4

Sens.: input sensitivity.
P.M.: phase margin.

2.2. InP HEMT ICs

We have developed 40-Gbit/s basic IC chip set using InP HEMTs. Fig. 2 shows the cross-sectional view of our 0.1-μm gate-length lattice-matched InAlAs/InGaAs/InP HEMT. The IC integrates HEMTs, InAlAs Schottkey diodes, metal resistors, MIM capacitors and two-level interconnection lines with a 2-μm-thick low-permittivity benzocyclobutene (BCB) interlayer. The InP gate-recess-etch stopper inserted into the InAlAs barrier layer drastically improves the uniformity of the threshold voltage (Vth) [5]. Typical average Vth is −0.5 V, and the standard deviation is low, around 13 mV for a 3-in. wafer. The typical transconductance (gm) is 1.2 S/mm, and the current gain cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) are 186 and 320 GHz, respectively.

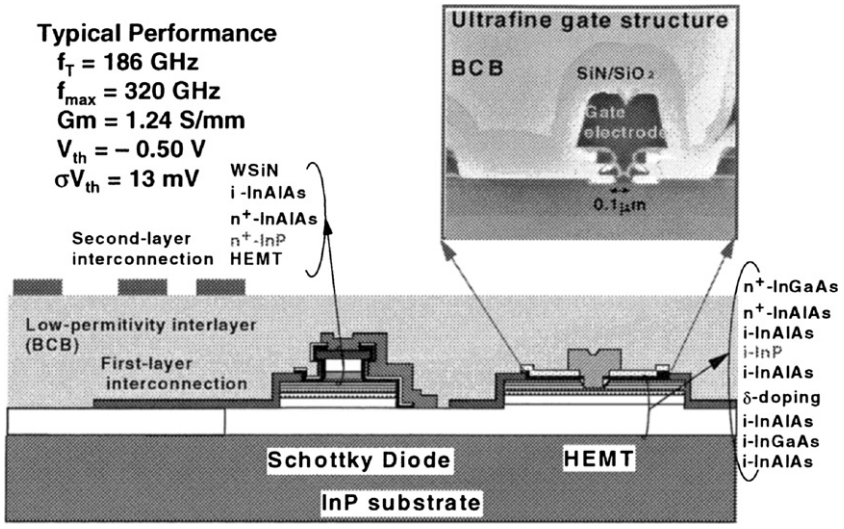

Fig. 2. Schematic cross-sectional view of the InP HEMT.

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