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A new way to selectively remove Si islands from polycrystalline silicon seed layers made by aluminum-induced crystallization

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Abstract

Polycrystalline silicon (grain size ~0.1–100 μm) solar cells on foreign substrates are a promising approach for the next generation silicon solar cells. Aluminum-induced crystallization AIC in combination with epitaxy is a possible way to obtain such absorber layers. It is believed that Si islands present on the surface of AIC seed layers have a negative effect on the epitaxy. The removal of these islands could therefore lead to an increased absorber layer quality and solar cell performance. In this paper, we present a selective island removal procedure based on the Al layer already present after AIC annealing. By selecting an etchant which removes Si at least as fast as Al (in this paper plasma etching using SF_6), the Al layer acts as a perfectly aligned etching mask for the fully developed islands.

Keywords: Aluminum-induced crystallization; Si island; Polycrystalline silicon; Thin-film solar cell; Selective etching

1. Introduction

The large growth of the photovoltaic (PV) energy market during the last ten years has resulted in a scarcity of high-quality silicon material and an increase of its price. Thin-film polycrystalline silicon (pc-Si) solar cells on foreign substrates might become a low-cost alternative for wafer-based silicon solar cells if sufficiently high efficiencies are obtained [1]. Direct deposition of Si on foreign substrates typically results in absorber layers with small grain sizes (0.2–1 μm) and a relatively high density of defects due to grain boundaries. To improve the electrical quality, a possible approach is the formation of a large-grained seed layer (1–100 μm) in combination with epitaxial growth. At IMEC an increase in absolute efficiency of ~1.5% per year up to 8% at the moment was achieved for pc-Si solar cells made by aluminum-induced crystallization (AIC) of amorphous silicon and thermal CVD [2]. The AIC seed layer itself can not be used as absorber layer due to its high p-type Al doping level of $\sim 3\times10^{18}$ cm^{-3} and due to the difficulty to make AIC layers with a thickness above 0.5 μm.

To obtain highly efficient pc-Si solar cells however, the material quality has to be further optimized and different cell processes have to be developed. On top of a typical AIC seed layer, secondary silicon crystallites (secondary crystallites with vertical side walls and a smooth upper surface are also called Si islands) are present after crystallization [3]. In the past we showed that an increase of the grain size (and removal of these secondary crystallites) of the AIC seed layer before epitaxy, does not necessarily lead to an increase in solar cell efficiency [4]. Recently, we showed that this was due to the presence of a very high density of electrically active intragrain defects [5]. These intragrain defects are a major limiting factor for the cell performance and therefore need to be reduced in number. From defect etching and electron backscattered diffraction (EBSD) measurement we concluded that most of these defects originate in the seed layer or at the seed layer/epi layer interface [5,6]. Despite the fact that removal of the secondary crystallites does not always lead to a better layer quality [4,5], we believe that their presence on the surface of the AIC seed layers has a negative effect on epitaxy, and/or will limit a further improvement of the absorber layer quality. Most Si islands have a

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different orientation compared to the underlying seed layer which can give rise to extra grain boundaries in the absorber layer (as we will show in this paper). Furthermore, the presence of Si islands makes the starting surface for epitaxy quite rough, which is known to be detrimental for the quality of the epitaxy.

In the past, different approaches were already proposed to remove the secondary crystallites (Si islands) on AIC seed layers [4,7–9]. Some of these methods need a change in the AIC process, while others are relatively difficult to implement. In this paper we present a new method which is generally applicable to all AIC seed layers that have fully developed Si islands.

2. Experimental

To withstand the high temperature needed for thermal CVD, alumina ceramic substrates (CoorsTek ADS996) with a RMS surface roughness of around 130 nm or glass-ceramic substrates with a RMS surface roughness of around 1 nm were used. Before AIC seed layer formation the surface of the alumina substrates was smoothed with a spin-on oxide (single Fox-25 layer with a final roughness of around 45 nm), which has a beneficial effect both on the seed layers (increasing grain size) and on the final solar cells (increasing Voc) [10]. After reducing the substrate roughness, a double layer stack of Al and a-Si was deposited in an electron-beam high vacuum evaporator. In between the two depositions, the aluminum layer was oxidized by exposure to air for 2 min. The nominal thickness of the Al and a-Si layers was fixed at 200 nm and 230–250 nm respectively. After deposition, the samples were annealed in a tube furnace under nitrogen ambient at 500° C for 4 h. During this annealing the a-Si crystallized into pc-Si and both layers exchanged places. The result is a pc-Si seed layer with a preferential (001) orientation and secondary silicon crystallites embedded in the Al layer on top of the pc-Si seed layer. When AIC seed layer were epitaxially thickened without secondary crystallite removal, the Al layer was removed by selective wet chemical etching. Before epitaxial thickening, samples were cleaned with a full RCA clean. Epitaxial growth was done in an experimental batch-type low pressure CVD system at a temperature of 1000° C [11].

Plasma etching used for island removal was done in a ML200RF reactive ion etching (RIE) system using O2 and SF6.

3. Results and discussion

In this section we will first give an example of the negative influence (extra grain boundaries) of Si islands present on the AIC seed layer during epitaxial thickening. Secondly, we present an island removal procedure that uses the Al layer around the Si islands as a perfectly aligned etching mask. Finally we present the first results of this new process, using plasma etching to remove the islands.

3.1. Epitaxial growth with islands present

Raman measurements showed that the Si islands formed during the AIC process were crystalline. In the past we already showed that the crystal orientation of these islands differs in most cases from the orientation of the underlying grains [12]. To experimentally confirm that islands can result in extra grain boundaries we have done high-resolution cross-section EBSD measurements of the silicon layer after epitaxial growth (at 1000° C using LPCVD). Fig. 1A and B are two inverse-pole figures (IPF) EBSD maps (250 × 440 points) with a step size of 20 nm. Fig. 1A represents the orientation along the growth direction (from the bottom of the figure to the top), and Fig. 1B represents the orientation in a direction perpendicular to the growth direction (perpendicular to the plane of the figure). The substrate is situated at the bottom in both maps. The vertical and horizontal resolutions differ in EBSD measurements (due to a tilt of the sample). The sample was mounted such that the highest resolution was obtained in the growth direction. Because no tilt correction was done on the IPF EBSD maps of Fig. 1, the grain width of the columnar grains looks more

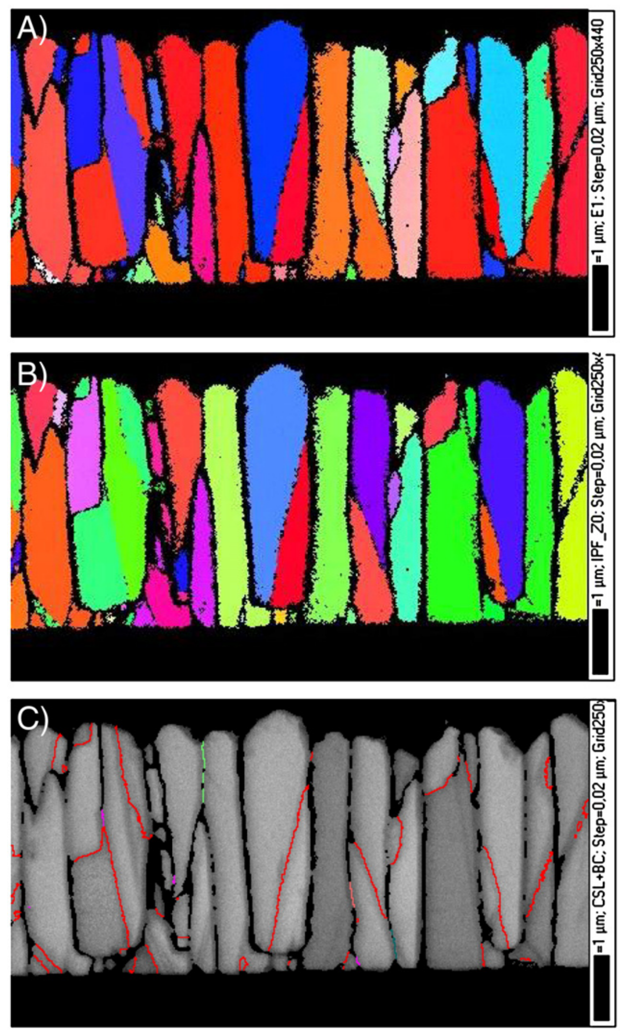

Fig. 1. Cross section EBSD measurement of an epitaxially thickened AIC seed layer using LPCVD at a temperature of 1000° C. A) IPF EBSD map representing the orientation along the growth direction. B) IPF EBSD map representing the orientation perpendicular to the growth direction (perpendicular to the plane of the figure). C) Coincidence site lattice boundaries (red color for Σ3) projected on top of the band contrast obtained during the EBSD measurement. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)