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Determination of bulk and interface density of states in polycrystalline silicon thin film transistors

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Abstract

The aim of our investigation is to determine the bulk and interface density of states in excimer laser annealed polycrystalline silicon thin film transistors (polysilicon TFTs). The exponential energy distribution of the band tail states in the bulk of the polysilicon layer is obtained from analysis of the space charge limited current in n^+–i–n^+ structures. The density of traps at the gate oxide/polysilicon interface and the slope of the exponential band tail states in a thin layer adjacent to the channel/gate oxide interface are extracted from low-frequency noise measurements. The experimental results indicate that the degree of disorder is improved in the upper part of the polysilicon layer due to its columnar growth.
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Keywords: Polysilicon TFTs; Bulk traps; Interface traps

1. Introduction

To improve the performance of polycrystalline silicon thin-film transistors (polysilicon TFTs), characterization of the quality of both interface between polysilicon/gate insulator and polysilicon bulk is needed. In n^+–i–n^+ sandwich structures, where the n^+ layer is used to inject carriers into the intrinsic (i) semiconductor layer, space charge limited currents (SCLC) were observed in amorphous silicon (a-Si) and used to determine the density of states in the bulk of the a-Si layer [1,2]. Since n^+–i–n^+ lateral structures are used in polysilicon TFTs, the drain current might also be space charge limited. In this case, SCLC measurements can permit to determine the density of states in the bulk of the polysilicon layer, since SCLC is not affected by the interface states.

In polysilicon TFTs, the origin of the low-frequency noise (LFN) is generally ascribed to carrier number fluctuations due to trapping and detrapping processes of free carriers in oxide traps located close to the gate oxide/polysilicon interface as in crystalline Si MOSFETs [3,4]. Recently, we have proposed a LFN technique to determine the density of the interface states and the slope of the exponential band tail states in the polysilicon active layer characterizing the degree of disorder of the material [5]. Because most of the channel conduction occurs in a thin layer adjacent to the channel/gate oxide interface, the extracted slope of the exponential band tail states characterizes the quality of the upper part of the polysilicon layer. In the present work, based on the combined analysis of LFN and SCLC measurements, we used analytical methods to determine the bulk and interface density of states in TFTs, showing that the degree of disorder in the upper part of the polysilicon layer is improved due to its columnar structure.

2. Experimental

Low-temperature polysilicon TFTs were fabricated on oxidized fused quartz glass substrates. The active polysilicon layer (50 nm thick) was prepared by solid-phase crystallization (SPC) at 600 °C for 24 h in nitrogen ambient of low-pressure chemically vapor-deposited amorphous silicon (a-Si) film, followed by KrF excimer laser annealing (ELA) with energy density 240 mJ cm^{-2}. Transmission electron microscopy analysis has shown that in the polysilicon films the average grain size is about 2500 nm with high in-grain defect density (about 5×10^{12} cm^{-2}) [4]. A standard self-aligned NMOS process was

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used to fabricate TFTs, with 120 nm thick SiO_2 gate insulator formed by electron cyclotron resonance plasma-enhanced chemical vapour deposition at 100 °C. Details for the device fabrication processes are presented elsewhere [4,5].

The current–voltage characteristics of the TFTs and n^+–i–n^+ structures were measured using a computer-controlled system including Keithley 617 electrometer and Keithley 230 voltage sources. Noise measurements in TFTs were performed at room temperature using a SR760 fast Fourier transform spectrum analyzer preceded by a low-noise current–voltage converter and a low-noise voltage amplifier. The devices were biased at various gate voltages and at 0.1 V on the drain for operation in the linear region. The gate and drain biases were supplied by CdNi batteries to reduce any external low-frequency noise.

3. Results and discussion

The transport properties of electrons in the bulk of the polysilicon layer are investigated by performing current–voltage (I–V) measurements in n^+–i–n^+ structures, formed between the drain and source contacts of the TFTs and with the gate electrode floating. An example of I–V curve of a typical TFT with gate width W = 50 μm and gate length L = 10 μm is presented in Fig. 1. In the I–V plot, two different regimes are distinguished. In the lower-voltage range (V < 5 V), the increase of the current with voltage is linear. At higher voltages, the current increases by many decades for a one-decade increase in voltage, following the power-law $I \sim V^m$ with m = 10.5. In Fig. 2, the experimental I–V characteristics of another set of n^+–i–n^+ structures are shown for W = 100 μm and different lengths L = 4, 7, 20 μm. The observed polysilicon length dependence of the current clearly proves that the electron transport is determined by the bulk-transport properties of the polysilicon layer.

The power-law voltage dependence of the current ($I \sim V^m$) is indicative of SCLC in the presence of an exponential distribution of traps in the bulk of the polysilicon layer [6]. For the exponential trap distribution described by

$$N(E) = N_t \exp\left(-\frac{E_c - E}{kT_t}\right), \tag{1}$$

the resulting SCLC is given by [7]

$$I = qA\mu_n N_c \left(\frac{2\gamma+1}{\gamma+1}\right)^{\gamma+1} \left(\frac{\gamma}{\gamma+1}\right)^{\gamma} \left(\frac{\varepsilon_s}{qN_t kT_t}\right)^{\gamma} \frac{V^{\gamma+1}}{L^{2\gamma+1}}. \tag{2}$$

Here A is the drain junction area, E is the energy from the conduction band edge E_c, N_t is the density of states at the conduction band edge, T_t is the effective temperature (inverse slope) of the trap distribution, q is the electronic charge, μ_n is the electron mobility, N_c is the effective density of states in the conduction band, ε_s is the dielectric permittivity of silicon, $\gamma = T_t/T$ and T is the measurement temperature. The slope of the log(I)–log(V) plot of Fig. 1 yields the characteristic energy of the trap distribution kT_t = 0.24 eV. Taking μ_n = 65 cm^2 V s^{-1} as obtained from analysis of the transfer characteristic of the TFT, it follows from Eq. (2) that $N_t = 7 \times 10^{17}$ cm^{-3} eV^{-1}. Using these parameters, we find good agreement between the experimental and theoretical results in the SCLC region, as shown in Fig. 1.

The density of the interface states and the slope of the exponential tail states in the polysilicon layer have been determined from analysis of LFN measurements [8]. For a typical TFT with the transfer characteristic presented in Fig. 3, noise measurements were performed at room temperature at drain voltage V_d = 0.1 V from weak to strong inversion exhibiting 1/f behavior. The 1/f noise has been employed to determine the density of traps at the polysilicon/SiO_2 interface. The experimental data of the normalized drain current spectral density S_I/I_d^2 versus I_d, measured at frequency f = 10 Hz, are presented in Fig. 4. Over the whole drain current region, Fig. 4

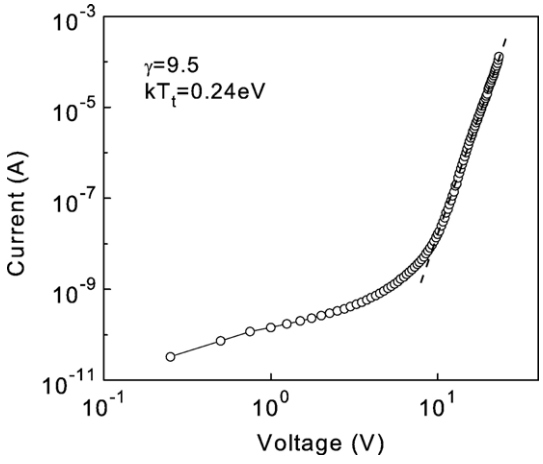

Fig. 1. Experimental (dots) and theoretical (dashed line) I–V characteristic, obtained from the n^+–i–n^+ structure of a polysilicon TFT with gate width W = 50 μm, gate length L = 10 μm and with the gate electrode floating. The polysilicon layer (50 nm thick) was prepared by SPC + ELA with laser energy density 240 mJ cm^{-2}.

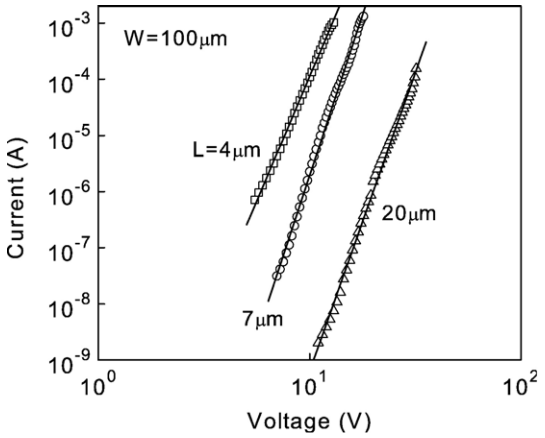

Fig. 2. Thickness dependence of the I–V characteristics, following the power-law of Eq. (2), obtained from n^+–i–n^+ structures of polysilicon TFTs with gate width W = 100 μm and gate lengths L = 4, 7 and 20 μm. The polysilicon layer (50 nm thick) was prepared by SPC + ELA with laser energy density 240 mJ cm^{-2}.

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