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Electric characteristics of organic thin-film transistors and logic circuits with a ferroelectric gate insulator

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Abstract

Organic electronic devices using a pentacene have improved importantly in the last several years. We fabricated pentacene organic thin-film transistors (OTFTs) with dielectric SiO_2 and ferroelectric $Pb(Zr_{0.3},Ti_{0.7})O_3$ (PZT) gate insulators. The organic devices using SiO_2 and PZT films had the field-effect mobility of approximately 0.1 and 0.004 cm^2/V s, respectively. The drain current in the transfer curve of pentacene/PZT transistors showed a hysteresis behavior originated in a ferroelectric polarization switching. In order to investigate the polarization effect of PZT gate dielectrics in a logic circuit, the simple voltage inverter using SiO_2 and PZT films was fabricated and measured by an output–input measurement. The gain of inverter at the poling-down state was approximately 7.2 and it was three times larger than the value measured at the poling-up state.

Keywords: Organic thin-film transistors (OTFTs); Ferroelectricity; Hysteresis; Inverter

1. Introduction

Organic materials such as pentacene and sexithiophene have attracted considerable attention due to their potentials for semiconductor's electronics [1–5]. Especially the characteristics of pentacene field-effect transistors (FETs) have made such devices feasible for applications requiring light weight, flexibility, low cost of fabrication, and solution processability. Pentacene is a well-known monomer as an organic semiconductor and has shown the field-effect mobility as high as 1.5 cm^2/V s in earlier works by Lin et al. [6]. However, the performance of organic thin-film transistors (OTFTs) was severely changed by the conditions of preparation process and the interface states between pentacene and insulator materials [7].

This paper reports on the morphological and electric properties of the pentacene thin-film transistors (TFTs). We also discuss the polarization effects of ferroelectric gate dielectrics on the device performance based on the results of drain current versus drain–source voltage (I_D–V_{DS}), drain current versus gate voltage (I_D–V_G), capacitance versus voltage (C–V), and output–input (V_{out}–V_{in}) measurements, *etc*.

2. Experimental

The pentacene thin films were deposited in situ on SiO_2 (300 nm)/Si and $Pb(Zr_{0.3},Ti_{0.7})O_3$ (PZT, 300 nm)/Pt(100 nm)/Ti(10 nm)/TiO_2(120 nm)/SiO_2(300 nm)/Si substrates by using a conventional thermal evaporator at the pressure below 10^{-6} Torr. The SiO_2/Si substrate was a heavily n-type doped and thermally oxidized silicon wafer. The ferroelectric PZT thin films were prepared on Pt/Ti/TiO_2/SiO_2/Si substrates by a sol–gel technique [8]. Pentacene materials were purified using the vacuum sublimator at 10^{-3} Torr or lower. The deposition rate of pentacene was about 1 Å/s and the substrates were maintained at 70 °C during the deposition. The thickness of pentacene was approximately 100 nm. The surface morphology of the films was examined by an atomic force microscopy (AFM). The ferroelectric properties of the PZT gate dielectrics were measured by using a Sawyer–Tower circuit and an impedance analyzer (HP4194A). The characterization of the OTFTs was conducted at room temperature using a semiconductor parameter analyzer (HP4145B) at various gate and drain voltages. By integrating two OTFTs in a

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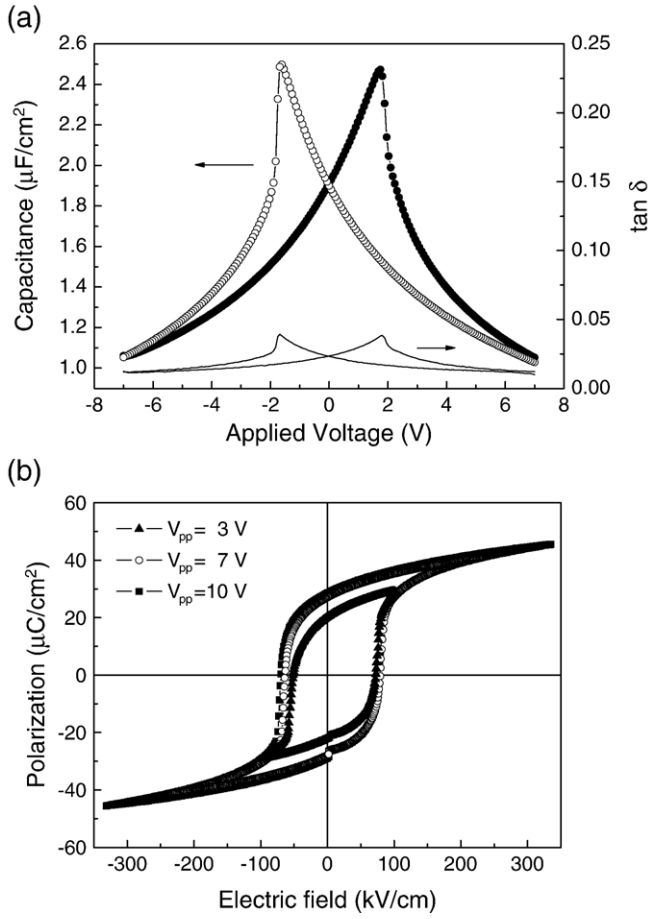

Fig. 1. (a) Capacitance and dissipation factor versus voltage characteristics, and (b) ferroelectric D–E hysteresis loops of a 300-nm-thick PZT film.

circuit configuration such that one of them was acting as a voltage-controlled switch, i.e. a driver transistor, and the other as an active load transistor, a simple voltage inverter was made. The driver and load transistors were the OTFTs with SiO_2 and PZT gate dielectrics, respectively.

3. Results and discussion

To investigate the ferroelectric domain switching and polarization reversal properties of 300-nm-thick PZT gate dielectrics, the C–V curves and the ferroelectric hysteresis (D–E) loops were measured. Fig. 1(a) shows the C–V and dissipation factor versus voltage (tan δ–V) curves. The area of a Pt/PZT/Pt capacitor was 5.3×10^{-4} cm^2. The amplitude and frequency of a small signal AC voltage were 100 mV and 10 kHz, respectively. The ramp rate was 0.5 V/s in both polarities. The peaks appearing at approximately −1.6 V and 1.75 V indicate clearly the ferroelectric polarization switching behavior. The difference in the intensity and the absolute position for the peaks originates in the different environments of the top and bottom electrodes, and differences in the work function, chemical composition, and stress. Fig. 1(b) illustrates the D–E loop measured using a sinusoidal voltage of 1 kHz with several amplitudes of 3, 7, and 10 V. The remnant polarization and the coercive field were approximately 29 μC/cm^2 and 78 kV/cm, respectively.

Topographic images of the pentacene films with a thickness of 100 nm deposited onto SiO_2/Si and PZT/Pt/Ti/TiO_2/SiO_2/Si substrates are shown in Fig. 2(a) and (b), respectively. The risen area that appears on the left side of each image is the pentacene film deposited onto a gold electrode. The inset of AFM image describes the schematic layout of OTFT structures. The topographic image was observed over the area of 5×5 μm^2 in a noncontact mode, and scan frequency was 0.5 Hz. The root-mean-square surface roughness values of pentacene/SiO_2, pentacene/Au/SiO_2, pentacene/PZT, and pentacene/Au/PZT were approximately 49, 38, 63, and 6 Å, respectively. The grain size of pentacene film grown on SiO_2 was larger than that on Au/SiO_2, but on the other hand the grains on the PZT and Au/PZT surfaces were almost similar in morphology.

Fig. 3(a) shows the typical plot of drain current I_D versus drain–source voltage V_{DS} at various gate voltages V_G for the pentacene TFT with SiO_2 gate dielectrics. The length and width of channel are 25 μm and 100 μm, respectively. The field-effect mobility, which was measured in the saturation regime due to the pinch off of the accumulation layer, was approximately

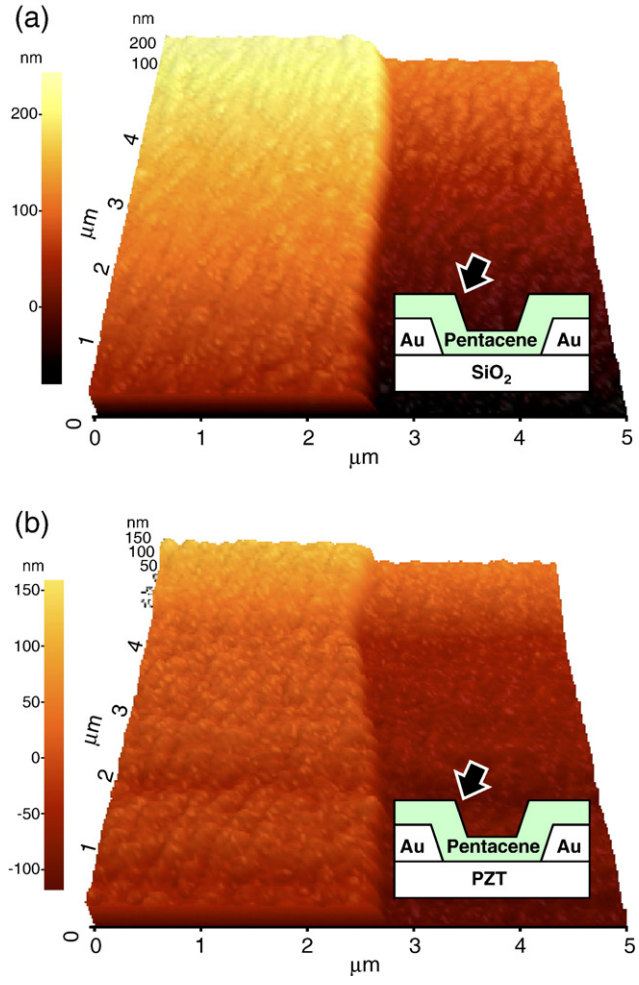

Fig. 2. Topographic images (5×5 μm^2) of the 100-nm-thick pentacene film deposited onto (a) SiO_2 and (b) PZT gate dielectrics. The risen area that appears on the left side of each image is the pentacene film deposited onto a gold electrode. The inset of AFM image describes the schematic layout of OTFT structures.