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Investigation of thermal stability of Mo thin-films as the buffer layer and various Cu metallization as interconnection materials for thin film transistor–liquid crystal display applications

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Abstract

Cu/Mo/Si multi-layer structures were fabricated to investigate diffusion behaviors and thermal stability between Cu and Mo. Physical vapor deposition (PVD), chemical vapor deposition, electroplating and electrolessplating were used to grow 100 nm thick Cu films as interconnection materials, and radio-frequency sputtering system was introduced to grow 37.5 nm thick Mo films as a buffer layer. All Cu/Mo/Si multi-layer specimens were annealed at 350 to 700 °C for 30 min. When the annealing temperature was over 600 °C, the Cu diffused through Mo into Si, and the Cu_3Si phase and Mo–Si intermetallic compounds formed at the Mo/Si interface. The diffusion mechanism is the grain boundary diffusion. The results indicate that Cu film deposited by PVD had best crystallinity, lower roughness, large adhesive energy and resistivity. The values of the resistivity, diffusion activity energy and large adhesive energy are 5.47 μΩ-cm, 0.948 eV and 2.46 N/m, respectively.

Keywords: Interconnection materials; Buffer layer; Intermetallic compounds; Boundary diffusion

1. Introduction

Thin film transistor–liquid crystal displays (TFT–LCDs) have become a mainstream in audio entertainment products, especially in large size TFT–LCD panels. This is due to being the small, thin and light, and having low power consumption. The length of the interconnection metals increases with the size of TFT–LCD panels. It becomes harder to maintain good uniformity of display quality, if the conventional Al or Cr metallization is applied. A good uniformity of display quality is based on sufficient charging at all the TFT array. The gate and data line delay are critical and the Resistance–Capacitance (RC) delay phenomenon become a concern. To overcome this issue, employing the suitable gate metal which has lower resistivity in TFT array fabrication is becoming a key technique [1,2].

Because of its lower resistivity (1.67 μΩ-cm) than Al (2.66 μΩ-cm) and better anti-electromigration resistance, Cu metallization has recently been considered more suitable to be an interconnection material than Al for applying in integrated circuits. This advantage can effectively reduce the RC delay phenomena and load a heavier current at the smaller areas. Furthermore, Cu intrinsically exhibit superior electromigration resistance compared to Al, and can improve reliability. Above all these advantages, Cu metallization has received considerable attention as a potential gate and interconnection materials in large size and higher resolution TFT–LCDs [3]. However, Cu may rapidly diffuse to Si to form the Cu_3Si phase and raise the electrical resistance, thus making the TFT array break down. Therefore, it is necessary to insert a suitable buffer layer between Cu and Si for the suppression of Cu diffusion.

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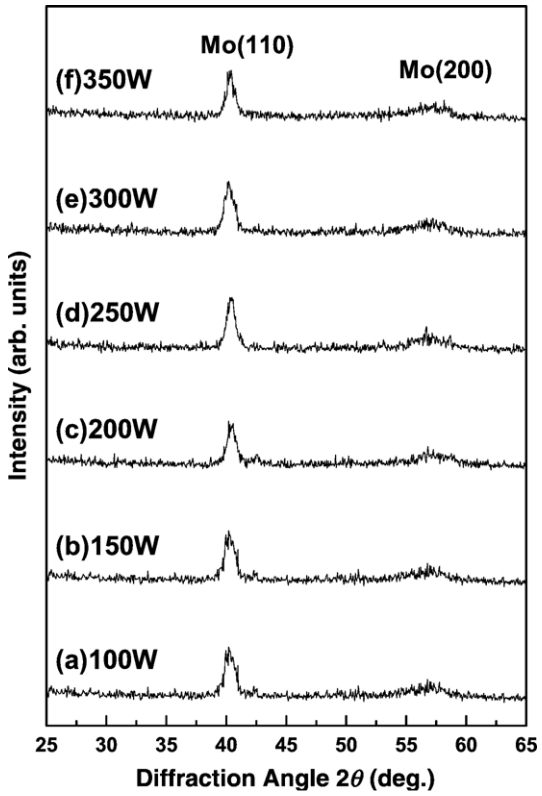

Fig. 1. XRD spectra of various deposited Mo films at various rf powers.

Mo has a high melting point (2623 °C), high thermal stability, good electrical-conductivity and a very low diffusivity. Among these advantages, the most important factor is that Mo has varied workability for the pattern fabrication. Line patterns or structures can easily be obtained from Mo by using dry or wet etching. Thus, Mo is considered to be a superior buffer layer material for Cu and Si. In addition, there are no intermetallic compounds between Cu and Mo while the temperature is below 1000 °C [4]. This implies that electrical resistance does not rise rapidly, as Cu and Mo come into contact. Although a lot of literature have been reported about interfacial phenomena between Cu and Mo or Mo-nitride [5–11], there is still some information lacking about the Cu/Mo/Si multi-layer structure. Thus, the applicability of Mo buffer layers to Cu-based interconnects should be urgently investigated.

Diffusion behaviors between Cu and Mo and the threshold mechanism are investigated in this study. Mo films are chosen to simulate a buffer layer in TFF–LCDs. RF sputtering system is introduced to grow 37.5 nm thick Mo films as a buffer layer. Physical vapor deposition (PVD), chemical vapor deposition (CVD), electroplating (EP) and electrolessplating (ELP) are applied to grow Cu film as interconnection metals. Sheet resistances and surface morphology of Mo or Cu films, diffusivity of Cu in Mo, threshold time of Cu/Mo/Si multi-layer and adhesive energy of Cu on Mo films were examined and determined, respectively. The purpose of this study is to compare these different deposition methods and to find out which is the best deposition method for Cu films to apply in TFT–LCD industries as interconnection materials.

2. Experimental procedures

2.1. Growth of Mo films

The substrate used in this study was an n-type (100) Si wafer with a resistivity of 1–10 Ω-cm. Prior to the loading into the sputtering chamber, the wafers were ultrasonically cleaned in acetone for 15 min, rinsed in de-ionized water for 15 min and then dipped in diluted HF solution for 1 min. Finally, the wafers were ultrasonically rinsed in de-ionized water for 5 min again to make sure that there were no contaminations on the Si surface. 37.5 nm thick Mo films were deposited by RF sputtering system. The base pressure was less than 1.2×10^{-5} Pa (1×10^{-7} torr), and the deposition pressure was kept constant at 6.7×10^{-1} Pa (5×10^{-3} torr). Several rf power scales, 100 W, 150 W, 200 W, 250 W, 300 W and 350 W were applied as the deposition parameter for Mo films growth. The crystalline structure of the Mo films was examined by cross-sectional transmission electron microscopy (XTEM). A JEOL 2000 FXII STEM (acceleration voltage of 200 kV) was used to examine samples which were prepared in a cross-sectional view. Film thickness was directly measured from the XTEM micrographs. X-ray diffractometer (XRD, Regaku RTP 300RC, Cu Kα radiation of $\lambda=1.5405$ Å) was used to examine the crystalline structure of Mo films and phase formation of the Cu/Mo/Si samples after annealing. The film resistivity was calculated from the sheet resistance measured by four-point probe (FPP, Napson RT-7) and the film thickness measured by XTEM. Surface morphology of the Cu/Mo/Si samples after annealing was characterized by SEM (JOEL JSM-6500F). Interfacial behavior was investigated by XTEM and X-ray photoelectron spectroscopy (XPS) depth profile. XPS was performed in Thermo VG Scientific Theta Probe spectrometer. All XPS data presented herein were acquired using a monochromatized Al Kα line 1486.6 eV. Peak positions were then calibrated with respect to the C 1s peak at 284.5 eV from the adventitious hydrocarbon contamination. For XPS depth profiling, 3 keV Ar+ ions were

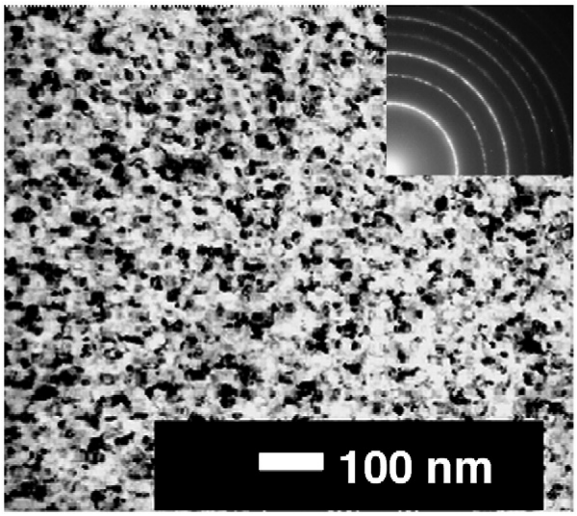

Fig. 2. Plane-view TEM bright field image and electron diffraction pattern of the Mo film deposited at a rf power of 250 W.