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Effect of thickness of ZnO active layer on ZnO-TFT's characteristics

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Abstract

We have investigated the electrical characteristics of ZnO thin film transistors with respect to the thickness of ZnO active layers. The ZnO layers with the thickness of 30 nm to 150 nm were deposited on bottom gate patterned Si substrate by RF sputtering at room temperature. The low-temperature oxide served as gate dielectric. As ZnO channel layer got thicker, the leakage current at $V_{DS}=30$ V and $V_G=0$ V greatly increased from 10^{-10} A to 10^{-6} A, while the threshold voltage decreased from 15 V to 10 V. On the other hand, the field effect mobility got around 0.15 cm^2/V s except for the 30-nm-thick channel. Overall, the 55-nm-thick ZnO channel layer showed the best performance.
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Keywords: ZnO; Thin film transistor; Thickness effect

1. Introduction

Nowadays, ZnO has been recognized as one of the most promising candidates for the next generation of transparent and flexible electronics for displays, such as thin film transistors on plastic substrates. Although, for the past 10 years, thin film transistors (TFTs) made by an amorphous or polycrystalline Si have been important elements in the flat-panel display industry, these TFTs (especially amorphous Si-TFTs) have such critical problems as light sensitivity and low mobility ($\leqq 1$ cm^2/V s) under light reduction. One approach to resolve these problems is to use the oxide semiconductor as a channel layer for TFTs. Recently, it has been suggested that intrinsic ZnO could be used as the active channel layer in the transistors, which utilize a transparent oxide semiconductor [1–6]. ZnO is one of the few oxides that can be grown as a crystalline material at relatively low deposition temperatures on various substrates including amorphous glasses and plastics. Furthermore, unlike amorphous Si TFTs and poly-Si TFTs, ZnO film with a wide direct bandgap of 3.4 eV, which does not degrade upon exposure to visible light, can also be employed to implement a channel layer for transparent TFT, so that there is no need to shield the active channel layer from visible light.

For TFT application of ZnO, one of the most important parameters is the on/off ratio. The good selection of on/off ratio should lead to low leakage current. Eq. (1) is a general form of leakage current ($I_{DS\ off}$) with respect to the thickness of the channel layer at TFTs, when the gate voltage V_{GS} is 0 V.

$$I_{DS\ off} = \frac{\sigma W t}{L} V_{DS} \tag{1}$$

where σ is the electrical conductivity, t is the thickness of channel layer, W and L are the width and length of the conduction channel, respectively, and V_{DS} is the source-drain voltage in the equation. According to Eq. (1), we need to optimize the thickness (t) of ZnO channel layer to reduce leakage current.

In this article, we thus investigate the characteristics of ZnO-TFT with respect to the thickness of the channel layers, and try to find the optimum thickness of the ZnO channel layer. For this purpose, the ZnO active layers were deposited using RF sputtering at room temperature with changing the thickness from 30 nm to 150 nm.

2. Experiment details

In our experiments, we employed bottom-gate and bottom-contact type TFTs. Fig. 1 shows a schematic cross-sectional view of our ZnO-TFT. Starting with a Si (100) substrate with

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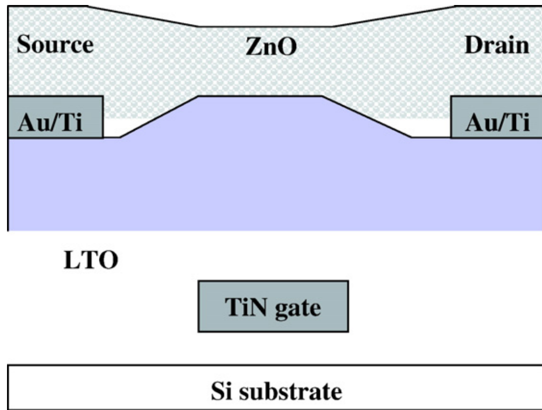

Fig. 1. Cross-sectional schematic diagram of the ZnO-TFT.

5-nm-thick TiN gate electrode formed by photolithography, 300-nm-thick low-temperature oxide (LTO) was deposited by LPCVD at 400 °C as a gate insulator. In the LTO growth process, we used SiH_4 and O_2 as the source of silicon and oxygen, where their mass flow in during growth was taken to be 160 sccm and 260 sccm, respectively. Source and drain electrodes, 50-nm-thick Au/Ti layers, were deposited by e-beam evaporation and defined by photolithography with liftoff. The device we measured has a channel width (W) of 250 µm and channel length (L) of 50 µm. Fig. 2 shows the optical image and AFM image of the TFT. The ZnO channel layers were deposited using RF sputtering at room temperature. The target was a ZnO (4 N) and sputtering gas was Ar. The pressure of the chamber before deposition was 10^{-5} Torr. RF power was 200 W, the flux of Ar gas was 70 sccm and the pressure of chamber was 7 mTorr in the deposition. The time of deposition was varied between 5 min, 10 min, 15 min, and 20 min. The thickness of the film was measured by the alpha step (Dektak 3st). ZnO film was annealed by furnace in N_2 ambient at 300 °C for 2 h after the deposition. The structural properties of ZnO films were investigated by atomic force microscopy (AFM), X-ray diffraction (XRD), and transmission electron microscopy (TEM) and the electrical characteristics of ZnO-TFTs were measured using a semiconductor parameter analyzer (Agilent 4155C).

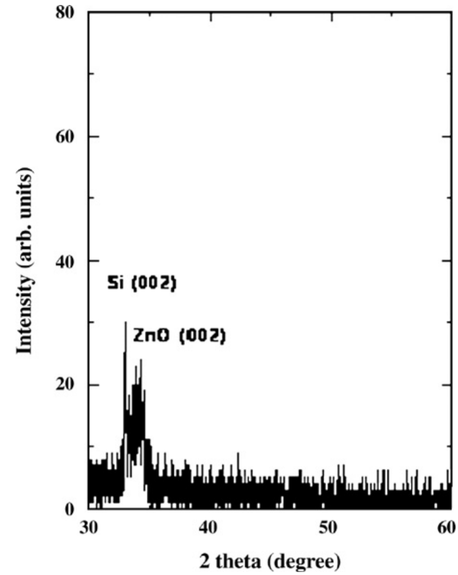

Fig. 3. XRD pattern of the ZnO film deposited at room temperature.

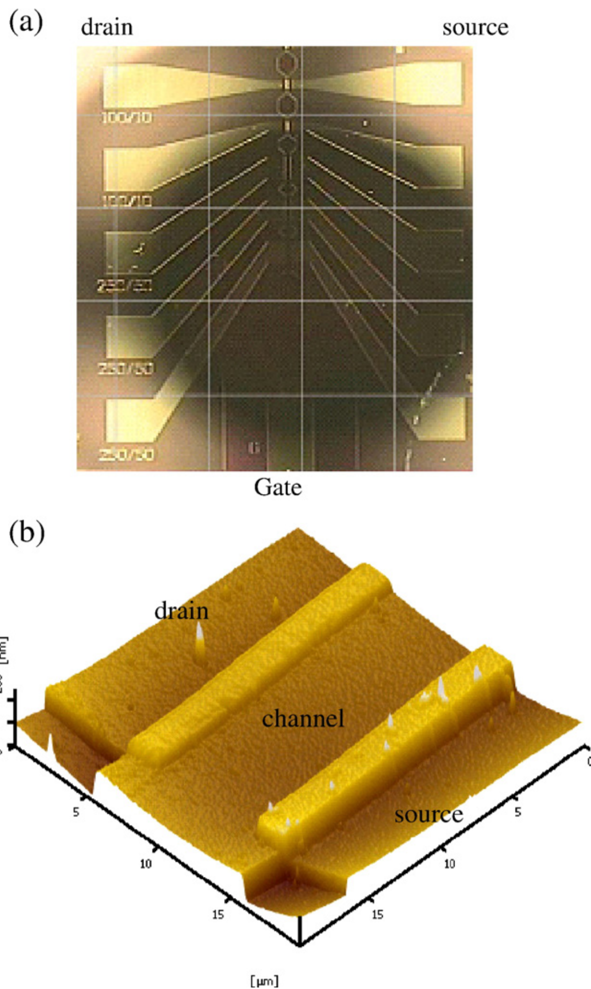

Fig. 2. (a) Optical image and (b) AFM image of the ZnO-TFT.

3. Results and discussion

Fig. 3 shows the θ–2θ XRD patterns of an *as-dep* ZnO film formed by sputtering at room temperature. Here, we can see two peaks, one peak of 34.4°, which corresponds to the (002) plane of the hexagonal ZnO crystal structure, and the other sharp peak

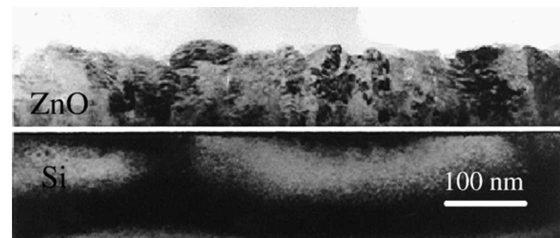

Fig. 4. Cross-sectional TEM images of ZnO films deposited at room temperature.

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