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Stressing effects on the charge trapping of silicon oxynitride prepared by thermal oxidation of LPCVD Si-rich silicon nitride

H.Y. Choi [a,*], H. Wong [a], V. Filip [a], B. Sen [a], C.W. Kok [b], M. Chan [b], M.C. Poon [b]

[a] Department of Electronic Engineering, City University of Hong Kong, Tat Chee Avenue, Kowloon, Hong Kong
[b] Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong

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Abstract

It was recently found that the silicon oxynitride prepared by oxidation of silicon-rich silicon nitride (SRN) has several important features. The high nitrogen and extremely low hydrogen content of this material allows it to have a high dielectric constant and a low trap density. The present work investigates in further detail the electrical reliability of this kind of gate dielectric films by studying the charge trapping and interface state generation induced by constant current stressing. Capacitance–voltage ($C-V$) measurements indicate that for oxidation temperatures of 850 and 950 °C, the interface trap generation is minimal because of the high nitrogen content at the interface. At a higher oxidation temperature of 1050 °C, a large flatband shift is found for constant current stressing. This observation can be explained by the significant reduction of the nitrogen content and the phase separation effect at this temperature as found by X-ray photoelectron spectroscopy study. In addition to the high nitrogen content, the Si atoms at the interface exist in the form of random bonding to oxygen and nitrogen atoms for samples oxidized at 850 and 950 °C. This structure reduces the interface bonding constraint and results in the low interface trap density. For heavily oxidized samples the trace amount of interface nitrogen atoms exist in the form of a highly constraint SiN_4 phase and the interface oxynitride layer is a random mixture of SiO_4 and SiN_4 phases, which consequently reduces the reliability against high energy electron stressing.

Keywords: Silicon oxynitride; Interface trap; Insulator trap; Oxidation

1. Introduction

Silicon oxynitride (SiO_xN_y) has been identified to be a better gate dielectric for replacing SiO_2 in deep submicron MOSFETs and advanced nonvolatile memory devices because of its enhanced robustness to high field and hot carrier stressing and large resistance against dopant (boron) penetration. Silicon oxynitride further offers a higher dielectric constant than conventional SiO_2 [1,2]. Due to the wide range of tunable refractive index, silicon oxynitride has also been used for fabricating Si-based optical waveguide devices [3]. Thermal nitridation of SiO_2 (or Si) in NH_3 or N_2O or NO has been widely used to grow oxynitride films [4–13]; however this method has some drawbacks, such as introduction of highly dense electron traps in the case of NH_3-based nitridation due to hydrogen incorporation, or lower amount of nitrogen incorporation in cases of N_2O and NO nitridation. It was found recently that the silicon oxynitride prepared by oxidation of silicon-rich silicon nitride (SRN) has several merits: it produces high nitrogen content (and thus a higher dielectric constant) and extremely low hydrogen content (and thus a lower trap density). Besides, interfacial nitrogen will exist in the form of random bonding to silicon and oxygen, which means a low defect density [14–16]. This paper presents a study on the stressing effects on the charge trapping properties of silicon oxynitride prepared by thermal oxidation of SRN. The experimental details will be given in next section and the results of high-frequency $C-V$ measurements after constant current stressing will follow in Section 3.

2. Experiment

The starting materials were p-type <100> silicon wafers. After the standard cleaning process, thin SRN layers were first deposited by low-pressure chemical vapor deposition (LPCVD) at a temperature of 780 °C. In order to study the bulk structure and properties of the oxynitride film and to avoid

* Corresponding author. Tel.: +852 92329717.
E-mail address: james0077hk@yahoo.com.hk (H.Y. Choi).

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the direct tunneling effects during the capacitance–voltage measurement and current stressing [5], thicker films were used in the investigation. The thickness of the deposited SRN layer was about 13 nm. The as-deposited SRN was then oxidized at temperatures of 850, 950, or 1050 °C for 1 h to form the oxynitride film. After oxidation, no pronounced increase in the thickness of the dielectric film was observed for the samples oxidized at 850 or 950 °C; but for the sample oxidized at 1050 °C, the Si-rich nitride layer was almost completely converted into SiO_2 and this heavy oxidation resulted in a significant increase in the oxide thickness to about 18.5 nm [15]. A thick aluminum layer was then deposited onto the wafer and finally Al electrodes were patterned using a photolithography technique and a number of MOS capacitors in different sizes were formed.

High-frequency (1 MHz) capacitance–voltage ($C-V$) characteristics of the MOS capacitors with diameter of 190 μm were measured using the HP4284A Precision LCR Meter. Constant current stressing with positive bias at the gate was applied using an HP4156A Precision Semiconductor Parameter Analyzer. The $C-V$ measurement and the current stressing were repeated in turn until the dielectric experienced a soft breakdown. The range of gate voltage used for each of the four samples was chosen such that the applied electric field was close to the soft breakdown (before stressing) of the sample. All measurements were carried out in a dark shielded chamber at room temperature.

3. Results and discussion

Fig. 1 shows the high-frequency (1 MHz) $C-V$ characteristics of the four samples before stressing. It was found that the $C-V$ curve (flatband voltage) shifts towards the negative side as the oxidation temperature increases because of the removal of excess Si atoms (≡Si–Si≡) which are diamagnetic defects in silicon nitride [2,7]. As the oxidation temperature increases (more effective oxidation), more excess Si atoms will be oxidized. As a result, more net positive charges turn out and thus produce a larger negative shift of the $C-V$ curves. On the other hand, it is also noted that, as the voltage sweeps from the accumulation region to inversion region, the $C-V$ slopes for the as-deposited sample and for the samples oxidized at 850 and 950 °C are essentially the same; whereas for the sample oxidized at 1050 °C, the slope is less steep indicating that the interface state density is higher than the other samples. This observation looks strange, as the Si/SiO_2 should have less interface states. It can be explained by the recently proposed interface bonding structure [13,16]. For the heavily oxidized sample, at 1050 °C, the SRN layer in the bulk was almost completely converted into SiO_2 and there was a considerably reduced amount of nitrogen at the Si/dielectric interface. A detailed X-ray photoelectron spectroscopy (XPS) study on the composition changed has been reported separately [16]. However, it was found that the trace amount of nitrogen at the interface is in the form of SiN_4 instead of the random bonding SiO_xN_y [13,16]. The phase separation effect (SiO_2 and Si_3N_4 phase) at high temperature (1050 °C) also leads to the formation of the over-constrained Si–N bonds [17] and hence brings a larger amount of interface traps.

One further interesting phenomenon is the increase of capacitance value in the strong inversion region as the oxidation temperature increases. This phenomenon is particularly obvious for the sample oxidized at 1050 °C. The capacitance value can increase up to ~65% of the insulator capacitance (C_{ox}). The rise in capacitance should be due to the increased charge trapping at high voltage. Because of the increased band bending at the interface in strong inversion regimes, the large amount of insulator traps in the gate dielectric can be filled with injected electrons, instead of saturating at the large forward bias. The interface states should also partly contribute to the high capacitance value at strong inversion.

Constant current stressing has a profound potential for studying the effects on the high-frequency $C-V$ characteristics. Fig. 2 displays the stressing effects on the high-frequency $C-V$ characteristics for two of the four samples. For the as-deposited sample, the flatband shift is insignificant for 200 s stressing at 24.5 $\mu A/cm^2$, indicating that the insulator trapping charge was insignificant at such a stressing level. However, at positive biasing of about 4 V, significant charge trapping was found as the stressing goes on. It is noted that the capacitance in the strong inversion region increases as the stressing proceeds. For the sample oxidized at 1050 °C, a progressive positive shift of the flatband voltage is found as the stressing proceeds because of the increasing electronic trapping, although the current density used for this stressing is only 7.0 $\mu A/cm^2$. After 400 s of stressing, the flatband voltage of 1050 °C sample reduces to a value closes to the 850 °C sample. When the voltage of the $C-V$ scans to more positive values, significant increases in the strong inversion capacitance are observed, due to the previously discussed interface and insulator traps charging effect. For the 950 °C sample, both the flatband shift and the inversion capacitance variation are minimal, suggesting that the oxynitride prepared in this condition is the best among the other samples.

Since the stressing current is generated at high fields (before the dielectric breakdown), the continuous bombarding of the Si/oxynitride interface with energetic electrons will cause the breaking of weak bonds (e.g. hydrogen bonds) in the region

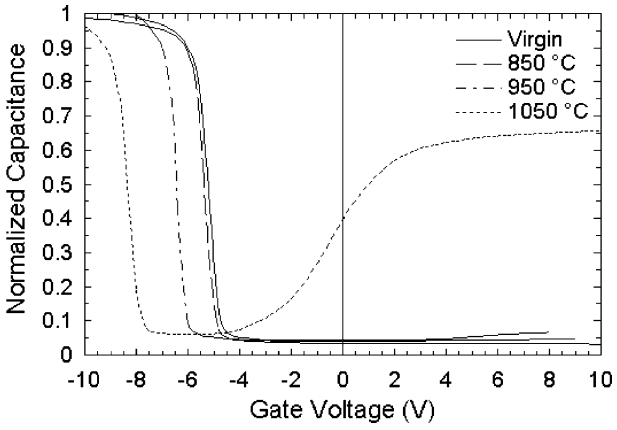

Fig. 1. High-frequency (1 MHz) $C-V$ characteristics of the samples before stressing.