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Localized germanium-on-insulator patterns on Si by novel etching scheme in CF_4/O_2 plasma

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Abstract

We report here a novel etch process scheme developed to form the Ge structures used in forming localized Ge on insulator (GOI) substrates. The approach of simultaneous etching the Ge film and photo resist provided greater advantages such as eliminating the necessity of post etch strip process step thus reducing process complexities and cycle time, over the conventional etch scheme. Various issues, which have shown up in the conventional etching, were also overcome. The etch process schemes are fully CMOS compatible and can be easily adopted for creating local regions of Ge on Si for advanced CMOS applications.

Keywords: Germanium etching; RIE of Ge; Etch schemes for Ge; Plasma etching of advanced materials

1. Introduction

Germanium is emerging as an important material to enhance the functionality of Si integrated circuits [1,2]. Recent advances in integrating Ge onto Si platform renews the interest in making use of the combination of its excellent electrical and optical properties [1–4]. The higher carrier mobility of Ge makes it attractive for high performance CMOS (especially with the prospect of high k gate dielectrics replacing SiO_2), and its high optical absorption at wavelengths important for communication applications makes it attractive for photo detectors. Through the development of methods to form local regions of Ge on Si, especially in the form of Ge on insulator (GOI) structures, integration of optoelectronic function with CMOS circuitry is gaining attraction [2,5].

To successfully integrate Ge onto a Si platform, material processing techniques suiting Ge need to be engineered. These processes include wet and dry cleaning/etching processes, thermal cycles and dopant activation. For integration schemes needing removal of Ge from unwanted regions of the wafer, etch chemistries need to be suitably identified. It is preferable to apply chemistries which are commonly used in CMOS technology. To achieve structural and dimensional control, dry etching techniques will be preferred over wet etching. As fluorides and chlorides of Ge are volatile species, the gases containing them will be of choice for technology applications.[6] Several gas mixtures such as SF_6 [6], $SF_6/H_2/CF_4$ [7], Cl_2/N_2 [8], SF_6/O_2 [9], have been investigated for different target applications. By-product layers such as sulphide and nitride have been observed in most of these studies.

In this work, we have evaluated Ge etch using CF_4/O_2 plasma with a less polymerizing gas mix ratio. Our objective is to achieve clean Ge surfaces at the end of the etch process scheme on locally defined regions of the Si wafer. In O_2-rich fluorine based plasma, formation rate of the volatile GeF_4 is expected to be high which provides high etch rates of Ge and also helps suppress polymerization. Various issues associated with Ge etching and resist stripping processes are identified

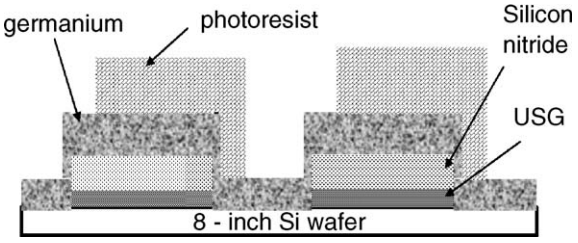

Fig. 1. Ge film stack (without hard mask).

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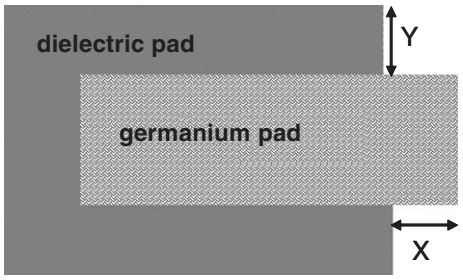

Fig. 2. Plan view of the final Ge pattern showing *X* and *Y* shifts.

and novel etch schemes with which clean and polymer free Ge surfaces can be obtained are demonstrated. This includes a hard mask scheme exploiting Ge etch process non-selective to photo resist.

2. Experimental details

In our experiments, 200 mm Si wafers were used as the starting material. A 15 nm thick SiO_2 was thermally grown on which Si_3N_4 was deposited by LPCVD. Patterning and etching were performed to form dielectric pads on top of the silicon surface. A 100 nm thick Ge film was sputter deposited on top of the patterned layer. Fig. 1 shows typical stack information used. Next a second patterning step was done with the first mask that had formed the dielectric pads at the first patterning step. However, pattern shifts were put to incorporate an *X* shift in the second patterning level with respect to the first. To take care of any misalignments in the *Y* direction, a pattern trim was also performed at both positive and negative directions to contain the Ge only on top of the dielectric pad in the rest of the area. This was done in order to create seeding windows where the Ge will be directly in contact with the silicon only at the window while the rest of the Ge will be on top of the dielectric pad. The final schematic (plan view) is shown in the Fig. 2. The purpose of this structure is to form GOI regions with open Si at one end to function as the seeding window for the liquid phase epitaxial growth of Ge [1,2].

Initially we evaluated Ge etching process by following a commonly used etch scheme viz., etch the Ge film and strip the resist to form the structures. Plasma etching of Ge was carried out in a medium density reactive ion etcher with a rotating dipole ring magnet (TEL-DRM). The resist stripping was carried out in another dedicated chamber. Post strip wet chemical cleaning was carried out in Verteq Gold-Finger single wafer process tool equipped with megasonic vibration capability.

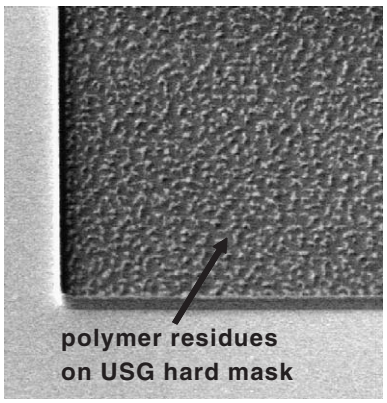

Fig. 3. Residues after plasma strip.

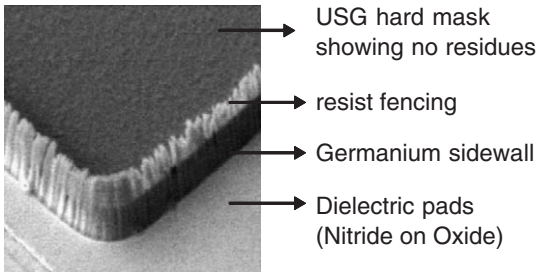

Fig. 4. USG hard mask with no residues on top and with resist fencing.

3. Results and discussion

Ge film was etched using CF_4/O_2 plasma with optimized gas flow rates of 40 and 20 sccm, respectively (ratio of 2:1) at 50 mT pressure with a plasma power density of ~3 W/cm^2. A moderate etch rate of 5000 Å/min was obtained. The Ge etch profile was close to vertical and etch selectivity of Ge to resist was close to 1. Post etch resist strip was performed using commonly used pure O_2 or H_2/N_2 plasma and it was found that Ge surface is completely damaged in both the strip plasmas.

3.1. Eliminating strip plasma exposure to Ge

To overcome this damage by eliminating the exposure of Ge surface directly to strip gas plasmas (such as O_2 and H_2/N_2), a hard mask layer of 100 nm thick un-doped silicon oxide (USG) was further added to Germanium (refer to film stack shown in Fig. 1earlier).

In the case of Ge etching with USG hard mask, photo resist stripping using the oxygen plasma result in complete removal of resist without adverse effect on Ge side walls (the only exposed areas to the strip plasma). However, polymer residues still exist on the USG hard mask, as shown in Fig. 3. These residues are found to be not removable by both amine and fluoride based wet chemical cleaning which are commonly used in CMOS fabrication technology for USG etch/strip processes [10]. However polymer residues were efficiently

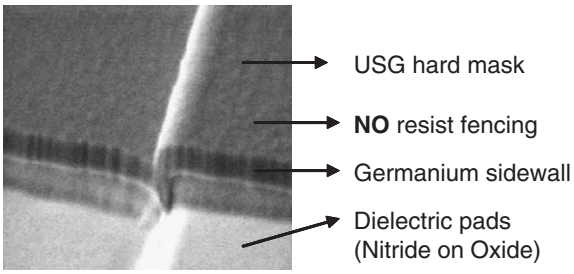

Fig. 5. Clean Ge structure with no resist fencing.