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Effect of silicidation on the electrical characteristics of polycrystalline-SiGe Schottky diode

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Abstract

Schottky diodes with good rectifying characteristics have been fabricated on the polycrystalline silicon–germanium (poly-$Si_{1-x}Ge_x$) thin film, deposited by the ion-beam-sputtering (IBS) technique. The influence of the Ge mole fraction and annealing condition on the electrical characteristics of a NiSi-Schottky diode grown on poly-$Si_{1-x}Ge_x$ film has been studied. NiSi-Schottky diodes are characterized in the temperature range of 125–300 K for the determination of Schottky barrier height (SBH), ideality factor (n), and interface–surface–grain-boundary state density (D_{it}). The current–voltage (I–V) characteristics have also been simulated in SEMICAD device simulator, by incorporating a modified poly-grain growth and mobility model of poly-SiGe material system to predict the effect of annealing temperature on the electrical properties of poly-$Si_{1-x}Ge_x$ Schottky diode.

Keywords: Schottky diode; Poly-SiGe; Interface state density

1. Introduction

Polycrystalline silicon–germanium (poly-SiGe) has emerged as a new (high performance) material for emitter in SiGe-HBTs (Heterojunction Bipolar Transistor) and advanced gate in complementary metal-oxide-semiconductor (CMOS) technology [1]. The fundamental electronic properties of poly-$Si_{1-x}Ge_x$ indicate that it can be a suitable alternative to poly-Si in microelectronic applications. Several potential uses for poly-SiGe have been recently reported and propose poly-SiGe a suitable alternative in Micro-Electro-Mechanical-System (MEMS) structures, CMOS technologies for improved trade-offs on mobility, and Thin Film Transistor (TFT) channel material for low temperature process technologies. Rapid thermal Chemical Vapour Deposition (CVD) has been employed to grow polycrystalline $Si_{1-x}Ge_x$ films [2], but the nucleation on oxide of thin polycrystalline film is rather difficult during this process. Only the low-pressure chemical-vapour deposition (LPCVD) technique produces a poly-SiGe film of much better quality at an elevated substrate temperature, which leads to a proper crystallization during the deposition process. Poly-SiGe alloys have a lower melting point than poly-Si, hence, physical phenomena like grain growth; changes in morphology with annealing, dopant activation, and diffusion are expected to occur at a lower temperature than in poly-Si. The above properties, together with the similarity of the electrical behavior of the polycrystalline materials, make poly-SiGe a suitable material for microelectronic applications where a low-thermal budget is required.

The understanding of solid-phase interaction between metals and poly-$Si_{1-x}Ge_x$ thin film has become important since poly-SiGe films are being used in the gate [3] and monocrystalline-SiGe in the source/drain [4] areas of MOSFETs for elevated source drain engineering. Moreover, conventional metal-gates are expected to replace poly-silicon gates in nanoscale MOSFETs in order to eliminate the poly-depletion effect, suppress boron penetration, and reduce gate resistance [5]. It is reported that, compared to Si thin film technology, poly-SiGe thin film uses a lower annealing temperature and shorter time, to form a low resistive silicide contacts. To the best of our knowledge, very little work has been done so far to study the effect of annealing on the electrical performances of metal/poly-SiGe contacts. However, in many potential applications, the contact properties of

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annealed structures are more important than those of an unannealed structure. For example, in an elevated source/drain MOSFET, the contact material on Si substrate is metal silicide, rather than metal itself. Recent reports show that self-aligned Ni-silicide has become almost indispensable in high-performance CMOS processing [6]. Besides, nickel has received major attention in submicron technologies as metal semiconductor contact, due to its low resistivity, chemical compatibility, low silicon consumption and thermal stability.

In this paper, we report on the influence of the Ge mole fraction and annealing condition on the electrical characteristics of a NiSi Schottky diode grown on poly-SiGe film. Poly-SiGe film is formed by solid phase crystallization of the amorphous SiGe layers with Ge mole fraction up to $x=0.1$–0.4. The effects of grain boundary deformation (with increasing Ge mole fraction) on the energy distribution of interface state density (D_{it}) have also been studied from the measured current–voltage and capacitance–voltage characteristics. Electrical characterization results of co-processed NiSi/Si and Ni-silicided/$Si_{1-x}Ge_x$ Schottky diodes are also compared.

2. Theoretical background and modelling

In poly-SiGe the potential barrier is small compared to poly-Si and the barrier height decreases with Ge mole fraction contributing to higher barrier width. As a result of this, the tunnelling component of current is very small for poly-SiGe Schottky diodes. Hence, one may neglect this tunnelling component and simulate the thermionic emission current density across the grain boundary by using following expression [7]:

$$J_{th} = \left(A^*T^2 q p_a\right)\exp\left(\frac{-q\phi_b}{kT}\right)\exp\left(\frac{q(V-jR_s)}{nkT}\right) \quad (1)$$

where $A^*=4\pi\ m^*k^2/h^3$ [7,8] is the effective Richardson constant, p_a is the average carrier concentration of the crystallite, m^* is effective mass of the carrier, T is the measuring temp in Kelvin, n is the ideality factor, V is the applied bias, ϕ_b is the effective barrier height and R_s is the series resistance associated with the diode. Modified Norde method [8] is used to extract the series resistance (R_s). Assuming thermionic emission as the main mechanism of current flow across the Schottky junction, Barrier height (ϕ_{b0}) can be calculated using the relation [9]

$$\phi_{b0} = \frac{k_b T}{q}\ln\left(\frac{AA^*T^2}{I_0}\right) \quad (2)$$

where A is the area of the diode and I_o is the saturation current. Similarly the ideality factor (n) is obtained from the relation [9]

$$n = \frac{q}{k_b T}\,\frac{\partial v}{\partial(\ln I)} \quad (3)$$

where $\frac{\partial v}{\partial(\ln I)}$ is the slope of linear extrapolated part of the forward current–voltage characteristics. Surface grain boundary or interface state density (D_{it}) of the Schottky junctions are determined from the measured low frequency (C_{LF}) and high frequency (C_{HF}) capacitances using the following expression [9,10]:

$$D_{it} = \frac{\varepsilon_i/\delta}{qC_{HF}}\,\frac{C_{HF}-C_{LF}}{C_{LF}-\varepsilon_i/\delta}\sqrt{q\varepsilon_s N_a/2\psi_s} \quad (4)$$

where ψ_s, δ and ε_i are the surface potential, thickness and permittivity of the interfacial layer, respectively. All extracted parameters are subsequently used in the analytical model for device simulation.

In this study, we propose a model to describe the grain boundary density and surface grain boundary states (D_{it}) for poly-SiGe Schottky diode. The I–V simulations at several conditions were performed using the SEMICAD device simulator [11]. In this simulator, the band gap reduction due to Ge concentration, lifetime of carriers, generation-recombination rate and the mobility of the carriers were incorporated as the major material parameters to describe the poly-SiGe material system. A mobility model has been developed for poly-SiGe, using hall mobility data, reported in Ref. [12] and subsequently incorporated in the device simulation to predict

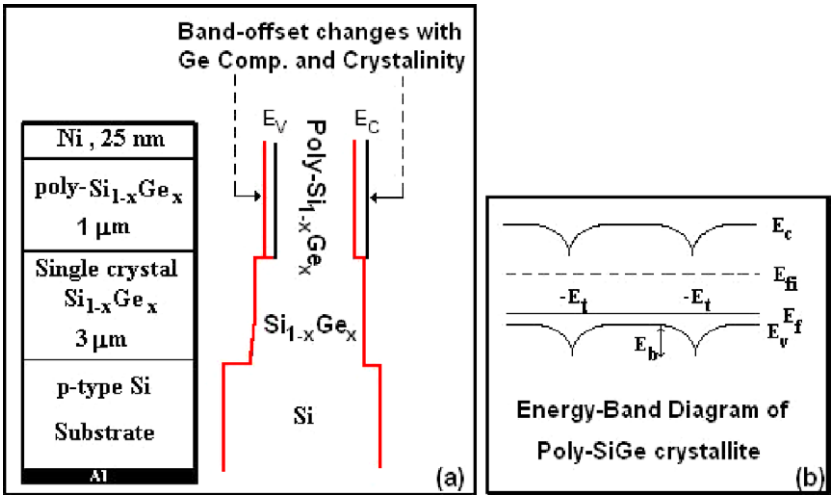

Fig. 1. (a). Schematic of a Ni-silicided/poly-$Si_{1-x}Ge_x$ Schottky diode. (b). Energy band diagram of poly-$Si_{1-x}Ge_x$ grains.