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Simulation of trapping properties of high κ material as the charge storage layer for flash memory application

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Abstract

We investigated the trapping properties of high κ material as the charge storage layer in non-volatile flash memory devices using a two-dimensional device simulator, Medici. The high κ material is sandwiched between two silicon oxide layers, resulting in the Silicon-Oxide-High κ-Oxide-Silicon (SOHOS) structure. The trap energy levels of the bulk electron traps in high κ material were determined. The programming and erasing voltage and time using Fowler Nordheim tunneling were estimated by simulation. The effect of deep level traps on erasing was investigated. Also, the effect of bulk traps density, thickness of block oxide and thickness of high κ material on the threshold voltage of the device was simulated.
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Keywords: SOHOS; Non-volatile memory; Traps; High κ

1. Introduction

The high-κ memory structure has drawn increasing attention in application for non-volatile flash memory device due to it's superior charge trapping properties compared to the conventional poly-silicon floating gate. The high κ material sandwiched between two silicon dioxide (SiO_2) layers to form the Silicon-Oxide-High κ-Oxide-Silicon (SOHOS) structure, stores charges in spatial deep level traps, making it less vulnerable to a single defect in the tunnel oxide. This significantly helps to minimize the discharge of the memory cell [1]. During the write (program) operation of the SOHOS n-channel transistor device, electrons tunneled through the tunnel oxide and are stored in the deep level traps [2]. During the erase operation under negative gate bias, electrons trapped in the high κ material are detrapped via tunneling through the oxide layer into the silicon substrate. However, there have been few reports for the trapping properties of the bulk traps in high κ material.

In this paper, we present the simulation results on the trapping properties of the high κ material as the charge storage layer in the SOHOS structure. The trap energy level of bulk electron traps in the high κ charge storage layer was determined. The programming and erasing voltage and time were explored. The effect of deep level traps on erasing is studied. Also, the effect of the trap density, thickness of the block oxide and the thickness of the high κ material on the threshold voltage of the device is investigated.

2. Device structure and model

2.1. Device structure

A schematic cross section of the SOHOS device used in the simulation is shown in Fig. 1. The gate stack consists of fours layers making up with a gate material of 4.6 eV, control oxide,

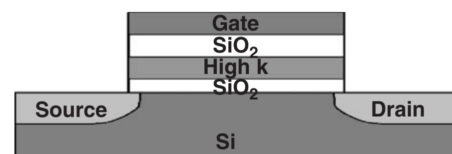

Fig. 1. A schematic cross section of the simulated SOHOS device.

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Table 1
Device dimension and doping concentration

Parameter	Value
Channel length(L)	0.16 μm
Control oxide thickness	4–26 nm
Tunneling oxide thickness	5 nm
High κ material thickness	5–10 nm
Substrate doping	1×10^{15} cm^{-3}
Source/drain doping	1×10^{20} cm^{-3}

high κ material and a tunnel oxide. The control and tunnel oxide material is SiO_2. The device dimension and doping concentration are given in Table 1. The properties of high κ material are shown in Table 2 [3].

2.2. Model in use

The simulator, Medici solves three partial differential equations self consistently for electrostatic potential, and electron and hole concentrations, using Poisson equation and the continuity equation. The modeling of the trapping and recombination of the traps are based on the Shockley–Read–Hall model. The programming and erasing mechanism considered in the simulation was Fowler Nordheim tunneling mechanism [4].

The change in threshold voltage, ΔV_{th} in continuous floating gate device like the SOHOS structure can be calculated as

$$\Delta V_{\mathrm{th}} = \frac{Q}{C_{d1+d2/2}} \tag{1}$$

where Q is the amount of charge stored in charge storage layer, $C_{d1+d2/2}$ is the capacitance of the block oxide and charge storage layer, $d1$ is the thickness of block oxide and $d2$ is the equivalent oxide thickness (EOT) of the charge storage area. The EOT of the high κ material can be calculated from

$$\frac{T_{\mathrm{highk}}}{\kappa_{\mathrm{highk}}} = \frac{EOT_{\mathrm{highk}}}{\kappa_{\mathrm{SiO_2}}} \tag{2}$$

where κ is the dielectric constant of the material and T_{highk} is the thickness of high κ material.

The control gate coupling ratio is given by [5]

$$\alpha_g = C_{cg}/\left(C_{cg} + C_{mos} + C_{fs} + C_{fd}\right) \tag{3}$$

where C_{cg} is the capacitance between the control gate and the charge storage layer, C_{mos} is the capacitance between charge storage layer and the channel, C_{fs} is the capacitance between the charge storage area and source and C_{fd} is the capacitance between the charge storage layer and drain. The change in threshold voltage can also be expressed as [6]

$$\Delta V_{\mathrm{th}} = V_{\mathrm{prog}} - \frac{1}{\alpha_g} T_{\mathrm{ox}} E_{\mathrm{f}} \tag{4}$$

where T_{ox} is the thickness of tunnel oxide and E_f is the electric field.

Table 2
High κ material properties [3]

Material	Dielectric constant (κ)	Bandgap E_G (eV)	ΔE_c (eV) to Si
SiO_2	3.9	8.9	3.2
Si_3N_4	7	5.1	2
Al_2O_3	9	8.7	2.8
Y_2O_3	15	5.6	2.3
La_2O_5	30	4.3	2.3
Ta_2O_5	26	4.5	1–1.5
HfO_2	25	5.7	1.5
ZrO_2	25	7.8	1.4

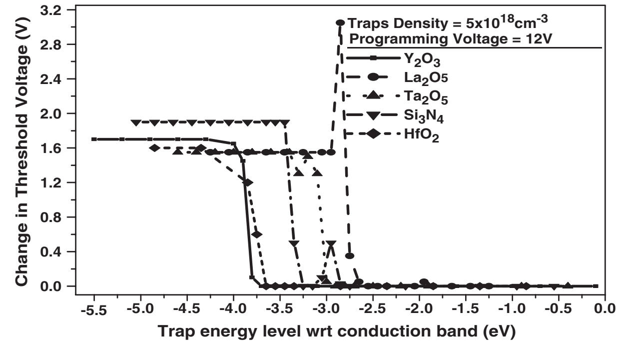

Fig. 2. Trap energy level of high κ material w.r.t conduction band.

3. Results and discussion

3.1. Trap energy level

The trap energy level of high κ material was simulated and it was observed that from Fig. 2, high κ material possesses deep level traps at around −4 eV from the conduction band, E_c. At such deep trap level, we can observe appreciable trap occupancy, resulting in change in threshold voltage, V_{th} due to the increase of electrons trapped in the charge storage layer. The trap occupancy plots for HfO_2 at different trap energy are shown in Fig. 3.

3.2. Trap density

Increasing the trap density increases the V_{th} as it allows increase in the amount of charges, Q stored in the device. The trap densities are increased from 1×10^{18} to 9×10^{18}cm^{-3}. This results in V_{th} of 0.9 to 3.6 V after writing at 12 V. Fig. 4 shows the increase in V_{th} after programming at 12 V for 10 ms.

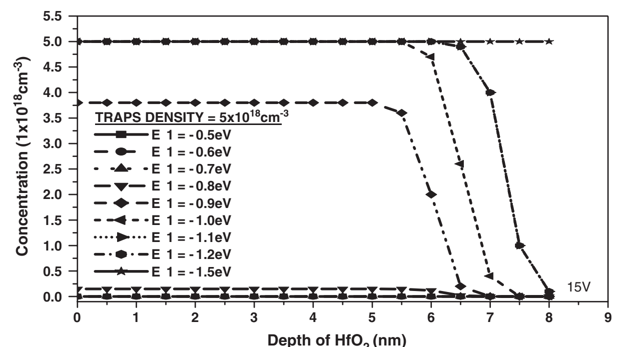

Fig. 3. Trap occupancy plots at different trap energy level for HfO_2.

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