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Effect of porosity and adhesion promoter layer on adhesion energy of nanoporous inorganic low-κ

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Abstract

A four-point bend technique (4PBT) was employed to characterize adhesion strength of nanoporous silica (SiCOH-based low-κ) to a hard mask layer (TEOS). Adhesion energy was analyzed as a function of low-κ porogen loading (3, 6, 9, and 11%). Effect of an adhesion promoter (AP) layer would also be discussed. Low fracture energies (< 5 J/m^2) confirm the weak mechanical properties of such highly porous materials. Fracture energy decreases as the porosity increases for samples without AP. However it becomes slightly higher and independent on the porosity when AP is applied. Low-κ/TEOS interface is the main delamination path for samples without AP. On the other hand, AP/TEOS interface becomes the interface that controls the adhesion for samples with AP hence it becomes independent on the low-κ porosity.

Keywords: Adhesion; Four-point bend; Porous low-κ

1. Introduction

As integrated circuit (IC) dimensions continue to decrease, RC delay, crosstalk noise, and power dissipation of interconnect structure become the limiting factors for ultra-large-scale integrated circuits. According to The International Technology Roadmap for Semiconductors 2004, as features sizes in IC approach 0.1 μm, it is necessary to reduce the dielectric constant of the dielectrics materials to below 2.2 [1]. This means these dielectric materials will need to be produced in a porous form. Due to the weak mechanical properties of the low-κ material, adhesion of the low-κ material to the surrounding layers become a critical issue for application consideration in the back-end-of-line especially when the dielectric material is highly porous [2].

2. Experiments

A layer of SiN (500 Å) was first chemically vapor deposited (CVD) onto Si substrate then followed by 6000 Å deposition of a nanoporous low-κ dielectric using spin-on-deposition. Porosity content was controlled by controlling porogen loading. The porogens are removed when the film is exposed to a bake sequence of 125, 200, and 350 °C for 1 min at each temperature. The samples were subsequently split into two parts, whereby half of them were coated with an 800 Å AP layer. Samples with and without AP were then cross-linked using a cure treatment of 425 °C for 1 h. Lastly, a 750 Å thick plasma enhanced CVD TEOS was deposited on all the films. The sample formation steps are illustrated in Fig. 1a and the schematic of the sample structure is shown in Fig. 1b.

The 4PBT specimens were made by cutting the wafers into rectangular specimens and creating a sandwich structure by bonding two rectangular pieces using a layer of passivating polymer (EpoTex™ 375). Note that the low-κ film was bonded to the back of the Si wafer so that there will be only one low-κ film at the middle of the sandwich. Great care was taken to keep the epoxy layer thin and

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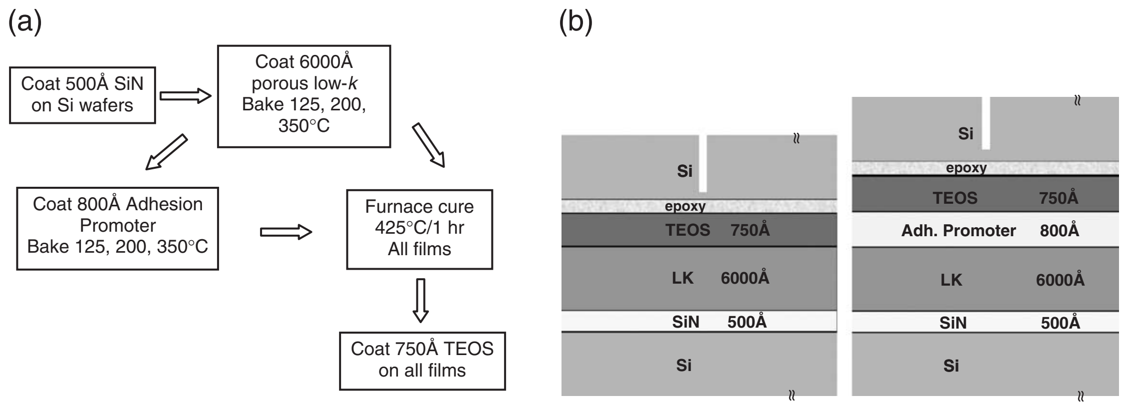

Fig. 1. (a) Sample fabrication process. (b) Sample structure with and without AP.

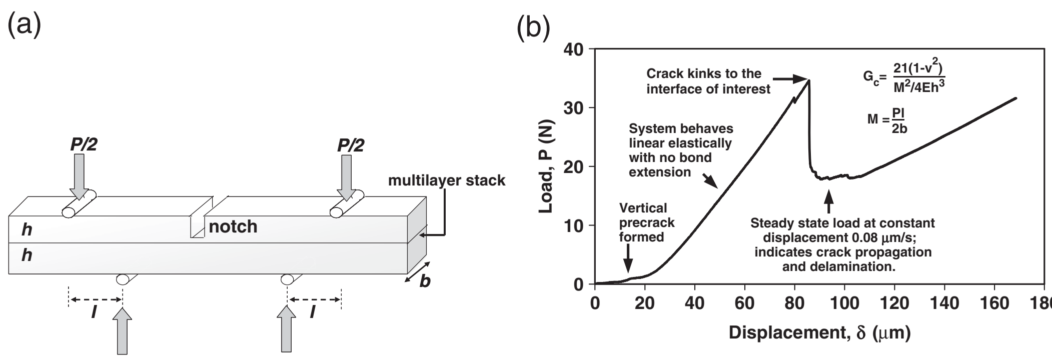

Fig. 2. (a) Experimental set up illustration for a simplified test structure. (b) A typical load vs. displacement curve obtained from 4PBT.

uniform and subsequently a weight was applied to ensure good bonding. The samples were then cured at 100 °C for 1 h and a notch was made on one side of the Si with a precision cutter as shown in Fig. 2a. The notch depth was 90% of the wafer thickness. Finally, the sample was centered between the four pins in the bend tester and loaded until it failed and the load versus crosshead displacement graphs were obtained.

3. Results and discussion

A typical load versus displacement curves obtained from the 4PBT is shown in Fig. 2b. Initially the load increases linearly as the specimen deforms elastically. At some point, the load decreases abruptly which signifies the point at which the vertical crack initiated by the notch begins to propagate through the Si. When it reaches an interface, it might be either deflected to propagate along the interface or continue through the next material in its vertical path. The crack takes the path that requires the least energy to overcome. Thus, the crack path would be determined by the adhesion at the interface and the toughness of the material ahead. When the film adhesion is poor, the crack is likely to propagate along the interface horizontally and then the load remains relatively a constant while the displacement increases. This plateau load is used to calculate the fracture energy, G_c, of the interface by Eq. (1) [3]:

$$G_c = 21\left(1 - v^2\right)M^2/4Eh^3 \quad (1)$$

$$M = Pl/2b \quad (2)$$

where E and v are the elastic modulus (= 169 GPa) and Poisson's ratio (= 0.28) of Si respectively, M is the net

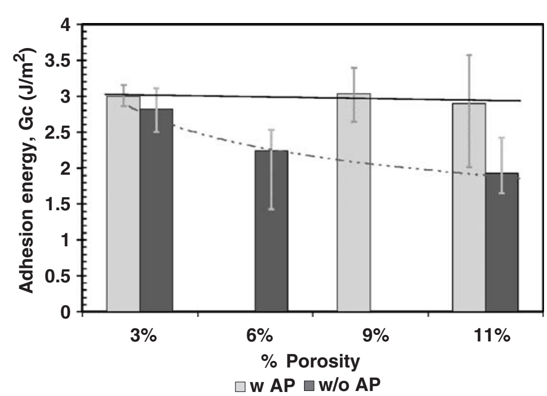

Fig. 3. Adhesion energy obtained from 4PBT vs. low-κ porosity for samples with and without AP.