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Study of gate leakage current in symmetric double gate MOSFETs with high-κ/stacked dielectrics

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Abstract

Quantum confinement in the ultra-thin silicon film of Double gate SOI MOSFETs affects the gate current (I_G). In this work, a systematic study on I_G in such devices for various high-κ/stacked gate dielectric material combinations with Equivalent Oxide thickness in the range of 1 to 2 nm has been carried out using a simulator developed for this purpose. The lower I_G in DG devices compared to bulk devices is attributed to reduced vertical electric field and quantum confinement effects. The amount of improvement is affected by the body thickness and the thickness of the gate dielectric. With higher value of κ, the reduction in I_G is even more pronounced. The gate dielectric can thus be more aggressively scaled with DG MOSFETs than with bulk-MOSFETs. It is found from our studies that Al_2O_3 is a better interfacial layer than SiO_2 and La_2O_3 is the most promising dielectric material to sustain scaling for the next decade.

Keywords: Gate leakage current; Double gate MOSFETs; High-κ dielectric

1. Introduction

The reduction of gate current (I_G) is an important reason for the intense research being carried out to replace SiO_2 with high-κ material in CMOS technology [1]. Table 1 lists a large number of high-κ dielectric materials which are being considered as prospective replacement for SiO_2 [1,2]. The suitability of a particular material not only depends on its dielectric constant (κ), but also on its conduction band offset to Si (ΔE_C) and its electron effective mass (m^*). An interfacial layer (IL) is generally found between the deposited high-κ layer and silicon substrate, creating a stacked dielectric. This layer can be an unavoidable silicate/oxide layer created during processing, or a layer which has been intentionally deposited/grown to improve the interface properties with silicon. A comparative study of I_G for various material systems would help to identify the ones which are most likely to replace SiO_2.

Recent studies on alternative CMOS device structures have shown that multiple-gate devices are ideally suited for ultimate CMOS scaling [3]. A Double-Gate (DG) MOSFET is composed of a thin silicon body sandwiched between the gate dielectrics and contacts. The two gates of the DG device are shorted giving rise to numerous advantages, such as greater control of the gate over the channel thereby reducing short-channel effects. Unlike bulk MOSFETs which require very high channel doping ($\sim 10^{18}/cm^3$ for sub-100 nm devices), thin body DG MOSFETs show good short-channel behaviour even with undoped silicon as channel. The two gates being at the same potential and a low channel doping makes the electric field in the direction normal to the Si–SiO_2 interface very low, resulting in low I_G. The advantages are enhanced by reducing the silicon film thickness. However, carrier confinement in MOSFETs with ultra-thin body (UTB) results in energy quantization. It is therefore necessary to carry out quantum-mechanical (Q-M) simulations to compute I_G in these devices. To the best of our knowledge, a Q-M simulator developed specifically to calculate I_G in DG MOSFETs with stacked gate dielectrics is reported for the first time in this paper. A simulation based study on I_G in DG MOSFETs has been reported earlier [4], but to obtain the potential profile it uses a general Schrödinger–Poisson solver, which does not consider wavefunction penetration into the dielectric. Also, the study [4] does not consider stacked gate dielectric. In this paper, the effect of the gate dielectric material as well as the silicon body

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Table 1
The bandgap (E_G), relative dielectric constant (κ) and conduction band offset with respect to silicon (ΔE_C) for various dielectric materials used in our simulations

Material	E_G (eV)	κ	ΔE_C (eV)
SiO_2	9.0	3.9	3.15
Si_3N_4	~5.0	7	2.0
Al_2O_3	8.7	9	2.8
Y_2O_3	5.6	15	2.3
La_2O_3	4.3	30	2.3
Ta_2O_5	4.5	~25	~1.4
TiO_2	3.5	~40	~1.1
HfO_2	5.7	25	1.5
ZrO_2	7.8	25	1.4

thickness on I_G is investigated. The leakage currents in DG and bulk MOSFETs are also compared.

2. Quantum-mechanical calculation of gate current in DG MOSFETs

Fig. 1 shows the energy band profiles along with the two lowest subband energy levels in a symmetrical DG Metal–Insulator–Semiconductor–Insulator–Metal (MISIM) structure with stacked gate dielectric. In an n-channel MOSFET, application of positive V_G increases the electron concentration in the channel and creates an inversion layer. The tunneling of electrons from the semiconductor channel through the gate dielectric results in gate current. In our calculations, we have taken the Si/SiO_2 interface to be parallel to the (100) plane, for which the conduction band is composed of six valleys, which split into two groups of subbands (known as ladders). The first set of subbands ($i=1$, unprimed ladder) is two-fold degenerate ($g_1=2$) and the effective mass in z-direction (normal to Si–SiO_2 interface) is given by $m^*_{z1}=m^*_l$(longitudinal electron mass)$=0.92m_o$, while for the second set ($i=2$, primed ladder), $g_2=4$ and $m^*_{z2}=m^*_t$ (transverse electron mass)$=0.19m_o$, where m_o is the electron free mass. In the simulator, at first the coupled Schrödinger and Poisson's equations are solved self-consistently without taking tunneling current into account. The potential variation obtained from this solution is then used to calculate the tunneling current. The Poisson's equation is given by

$$\frac{d}{dz}\left[\varepsilon(z)\frac{d\phi(z)}{dz}\right] = q\left[N_D^+(z) - N_A^-(z) - n(z) + p(z)\right] \quad (1)$$

where $\phi(z)$ is the electrostatic potential, $\varepsilon(z)$ is the spatially dependent permittivity, $N_D^+(z)$ and $N_A^-(z)$ are the ionized donor and acceptor concentrations, and $p(z)$ and $n(z)$ are the hole and electron concentrations. The Schrödinger equation is expressed as

$$\left[-\frac{\hbar^2}{2}\frac{d}{dz}\frac{1}{m^*_{zi}}\frac{d}{dz} + V(z)\right]\Psi_{ij}(z) = E_{ij}\Psi_{ij}(z) \quad (2)$$

where Ψ_{ij} is the normalized wave function of electrons for the confined energy level E_{ij} (which corresponds to the jth quantized energy level for the ith valley in the conduction band), $\hbar$ is the reduced Plank's constant and the potential energy $V(z)$ is related to $\phi(z)$ through $V(z)=q\phi(z)+\Delta E_C(z)$, where $\Delta E_C(z)$ is a pseudopotential energy due to the material dependent conduction band discontinuity with respect to Si. The subband energies are obtained from the eigenvalues of the Schrödinger equation. Both Eqs. (1) and (2) are discretized and solved using the Finite Difference Method (FDM). While V_G is used as the boundary condition for Poisson's equation, the Schrödinger equation is solved with closed boundary conditions, i.e., $\Psi_{ij}=0$ at the metal-dielectric interfaces. It is important to consider wavefunction penetration into the gate dielectric as this can lower the subband energies because carriers are no longer perfectly contained inside the potential well. The subband energy difference with and without consideration of wavefunction penetration can be as much as 10–20 mV [4] depending on the values of ΔE_C and m^*_{zi}. Thus, the subband energies are dependent upon the gate dielectric material. After obtaining $\Psi_{ij}(z)$ from the solution of Schrödinger's equation, $n(z)$ in the discretized energy levels in the 2-D electron gas (2-DEG) at the silicon surface can be obtained as [5]

$$n(z) = \frac{k_B T}{\pi\hbar^2}\sum_i g_i m^*_{di}\sum_j \ln\left[1+\exp\left(\frac{E_F - E_{ij}}{k_B T}\right)\right]|\Psi_{ij}|^2 \quad (3)$$

where k_B is the Boltzmann constant and $m^*_{d1}=m^*_t$ and $m^*_{d2}=\sqrt{m^*_l m^*_t}$. $p(z)$ is calculated classically using the Boltzmann relation. Thus, solution of Schrödinger equation leads to calculation of $n(z)$ and $p(z)$, which is then used to solve Poisson's equation, giving us the potential varaiation $\phi(z)$ and $V(z)$, which is again used to solve Schrödinger's equation. This process is continued till convergence is achieved. The potential profile obtained from the self-consistent solution of Schrödinger and Poisson's equations is used to calculate I_G. Since the two gates are shorted and the device is symmetric about the center of the silicon channel, the current for each gate is $I_G/2$. Thus, the tunneling probability can be calculated by considering one half of the device, which consists of the gate metal, the gate

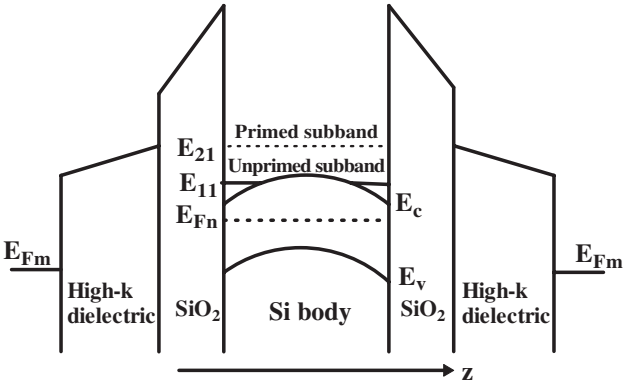

Fig. 1. Energy band diagram in a symmetric metal–insulator–silicon–insulator–metal (MISIM) structure. The two lowest subband energies are also shown.