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Study on electrical degradation of p-type low-temperature polycrystalline silicon thin film transistors with $C–V$ measurement analysis

Shih-Che Huang [a,*], Yu-Han Kao [a], Ya-Hsiang Tai [b]

[a] Department of Photonics & Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu, 300 Taiwan
[b] Department of Photonics & Display Institute, National Chiao Tung University, Hsinchu, 300 Taiwan

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Abstract

Laser recrystallized low-temperature poly-silicon (LTPS) films have attracted attention for their application in thin-film transistors (TFTs), which are widely used in active matrix display. However, the degradation behavior of p-type LTPS TFTs is not quite clarified yet. In this paper, the instability mechanisms of p-channel LTPS TFTs under DC bias stress have been investigated. From the IV transfer curves, it was observed that LTPS TFT's mobility increases after stress at some bias conditions. This degradation is most likely caused by interface traps between the poly-Si thin film and the gate insulator, as well as the damaged junction of the drain from stress. In this work, the assumption is examined via $C–V$ measurement. It is found that the C_{GD} curves of the stressed TFT slightly increase for the gate voltage smaller than the flat band voltage V_{FB}. However, the C_{GS} curves of the stressed device are almost the same as those before stress. By employing simulation, it is found that the degradation of p-type TFTs under this stress condition is mainly caused by the trapped charges at the interface between the gate and the drain region, which is generated by the high voltage difference applied during DC bias stress.

Keywords: Thin film transistor; Poly-Si; LTPS; p-type; $C–V$ (capacitance–voltage) measurement

1. Introduction

Low-temperature poly-Si (LTPS) thin film transistors (TFTs) have attracted much attention for AMLCD and AMOLED applications due to their high mobility and the capability of realizing integrated circuits on glass [1]. The reliability issues of the LTPS TFTs are of special importance in practical application. It was reported that poly-Si TFTs suffer from several degradation mechanisms, such as hot carrier effects [2–4], self-heating effects [5,6], water [7], and photon-induced leakage current [8,9]. For the reliability issues mentioned above, most of the previous works focused on the current transfer characteristics to investigate the mechanism of degradation after DC stress. Since the $I–V$ transfer curves show the overall behavior of the channel, it would be difficult to identify the degradation mechanism as well as the location of the damaged regions in the device. In this work, the DC bias tests were performed and the stressed TFT were examined with $C–V$ (capacitance–voltage) measurement. The capacitance C_{GS} between the source and the gate, as well as the capacitance C_{GD} between the drain and the gate, can be measured. The difference between C_{GS} and C_{GD} can reveal the locations of the damaged regions [10]. Besides, the frequency dependence of the $C–V$ curves help to identify whether the dominant mechanism of degradation is the increase of fixed charges or trap states.

2. Experiments

The process flow of TFTs is described below. First of all, the buffer oxide and a-Si:H film with thickness of 50 nm were deposited on glass substrates with PECVD. The samples were then put in the oven for dehydrogenation. The XeCl excimer laser of wavelength 308 nm and energy density of 400 mJ/cm^2 was applied. The laser scanned the a-Si:H film with a beam width of 4 mm and 98% overlap to recrystallize the a-Si:H film to poly-Si. After poly-Si active area definition, 100 nm SiO_2 was deposited with PECVD as the gate insulator. Next, the metal gate was formed by sputter and then defined. The p^+ source/drain doping was done by B_2H_6 self-align implantation with a dosage of 2×10^{15} cm^{-2}. Then, the interlayer of SiN_x was deposited. Subsequently, the rapid thermal annealing was

* Corresponding author.
E-mail address: hansley.eo92g@nctu.edu.tw (S.-C. Huang).

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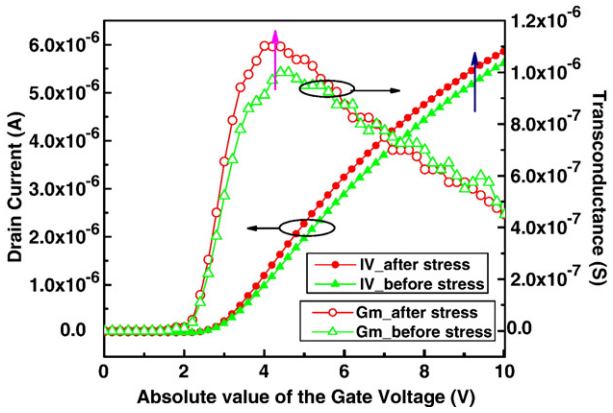

Fig. 1. I_d–V_g and transconductance curves before and after DC stress condition of V_g=−2 V and V_d=−20 V.

conducted to activate the dopants. Meanwhile, the poly-Si film was hydrogenated. Finally, the contact hole formation and metallization were performed to complete the fabrication work.

The Agilent 4156A semiconductor parameter analyzer was used to measure the I–V curve and stress the device at different conditions. The C–V curves of the gate-to-source capacitance (C_{GS}) and gate-to-drain capacitance (C_{GD}) before and after stress at different frequencies were measured with the Agilent 4284A precision LCR meter.

3. Results and discussion

In this study, the p-type TFTs with a channel width of 20 μm and a channel length of 5 μm were fabricated. These devices

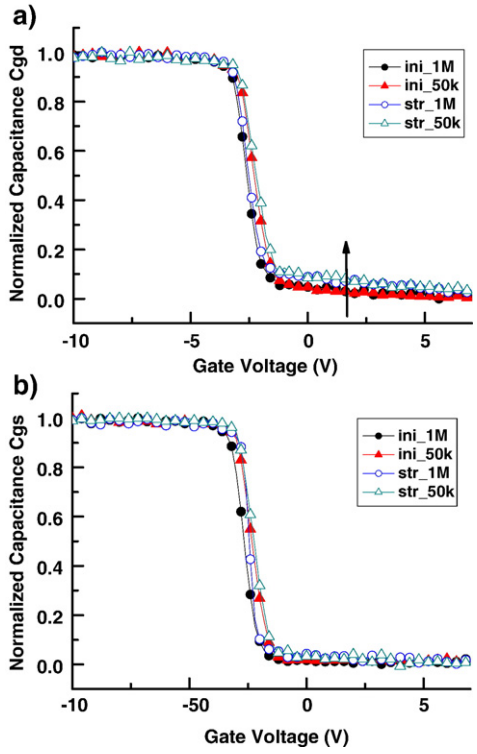

Fig. 2. (a) and (b). Normalized C_{gd} and C_{gs} curves (before and after DC stress) versus gate voltage at frequencies 50 K and 1 MHz.

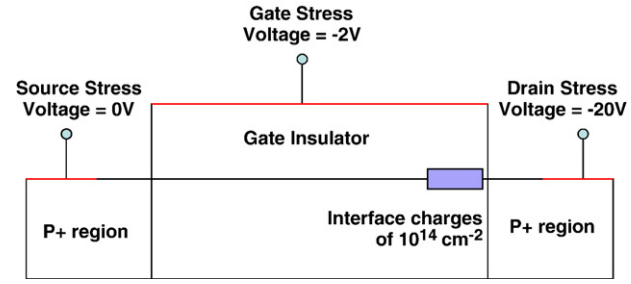

Fig. 3. The proposed degradation model in the TFT structure with interface charges.

were stressed at various conditions of the gate-to-source voltage V_{gs} and the drain-to-source voltage V_{ds} in the range of 0 V to −20 V. For most conditions, the threshold voltage V_{th} shifts negatively and the mobility degrades. These results are well explained in previous reports [11–13]. However, for certain conditions, especially that of V_{gs}=−2 V and V_{ds}=−20 V, the increase of TFT's mobility can be observed.

Fig. 1 shows the curves of the I–V transfer and transconductance Gm of the p-type poly-Si TFT before and after this particular stress condition. After stress, the on current shows a slight increase and a very small change in the threshold voltage and the subthreshold swing. However, the changes of the Gm curve are more obvious since the transconductance represents the derivative of the drain current via gate voltage. As shown in Fig. 1, Gm reaches its maximum at the gate voltage of −4 V and the maximum value increases about 15% compared to that before stress. For the gate voltage between −4 V and −10 V, the Gm curve of the stressed device also decreases more rapidly than that of the unstressed device.

Since the I–V transfer curves show the entire characteristics of the whole channel and may not distinguish the dominant mechanism, C–V measurements were further employed to investigate the asymmetry electric fields at the source and drain of TFTs during the stress. Fig. 2(a) shows the gate-to-drain capacitance C_{GD} curves before and after stress at different frequencies, while Fig. 2(b) shows the corresponding curves of the gate-to-source capacitance C_{GS}. The C_{GD} curves were measured with a floating source and C_{GS} curves were measured with a floating drain. The C–V curves were plotted with normalized value of capacitances, which is the ratio of the measured value to the maximum value of the measured capacitance.

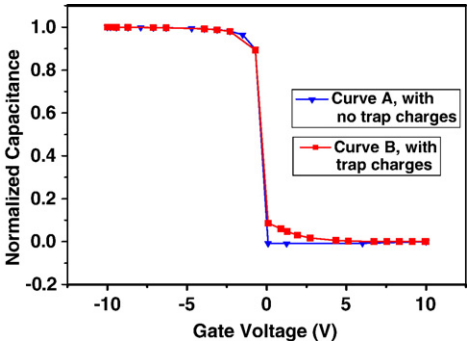

Fig. 4. Simulation results of the normalized C–V curves with and without