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Instability of threshold voltage under constant bias stress in pentacene thin film transistors employing polyvinylphenol gate dielectric

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Abstract

The instability of threshold voltage and mobility of pentacene thin film transistors using a poly(4-vinylphenol) gate dielectric have been investigated under constant bias stress. The mobility was very stable in vacuum by exhibiting 2% variation after 6 h stress even under the high gate bias stress of $V_{GS}=-20$ V. Meanwhile, we observe a negative shift of threshold voltage under stress in vacuum. This shift is attributed to charges trapped in deep electronic states in pentacene near the gate interface. We propose a model for the negative shift of the threshold voltage and extract the hole concentration, 4.5×10^{11} cm^{-2}, needed to avoid the onset of stress effects, resulting in a design rule of the channel width to length ratio larger than 40.

Keywords: Organic semiconductors; Stress; Threshold voltage shift; Interfaces; Electronic devices

1. Introduction

The technology of organic thin film transistors (OTFT) is approaching a mature stage, and is now applicable to backplanes for flexible displays and integrated circuits for radio frequency identification [1]. Pentacene is an organic semiconductor that can be utilized in high performance OTFTs [2,3]. For high performance, gate dielectric materials are also important as the properties of the organic semiconductor layer are largely determined by the gate.

Poly(4-vinylphenol) (PVP) is attracting attention as a gate dielectric material. It is considered to be especially suitable for pentacene, because it exhibits high insulation with a low leakage current density of 5×10^{-10} A/cm^2, and provides a good surface energy for pentacene molecular ordering [2]. It also can be deposited as a thin film at low temperature of less than 200 °C, thus enabling flexible applications [2]. For commercialization of a combination of PVP with pentacene, the stability issue must be addressed. However, the stability of OTFTs using a PVP gate in combination with pentacene has not been sufficiently addressed, in contrast with the abundance of stability reports on OTFTs using an SiO_2 gate.

Origins of OTFT degradation include hydroxyl radicals trapped at grain boundary [4,5], oxygen doping in the organic semiconductor [6–9], charge trapping at defect states at the interface or inside the insulator [10–14], water vapors in the insulator [12,15], bipolaron formation by accumulated holes [16], Na^+ migration in a glass substrate [17], leakage current through the gate dielectric [18], and electron trapping by a hydroxyl group on SiO_2 [19]. In response to concerns over the stability of organic semiconductors, most works in this area have used OTFTs employing an SiO_2 gate in the fabrication of control devices. However, the stability of OTFTs is not affected by the organic semiconductor alone but also by the gate material as well.

In this paper we investigated the stability of pentacene TFTs employing PVP as a gate dielectric. We have proposed a model to describe the threshold voltage shift under constant bias stress, and also extracted a criterion and a design rule of OTFTs to minimize the stress effect.

2. Experimental details

The OTFTs employ aluminum as a gate electrode, which was deposited and patterned on a glass substrate. PVP was then spin

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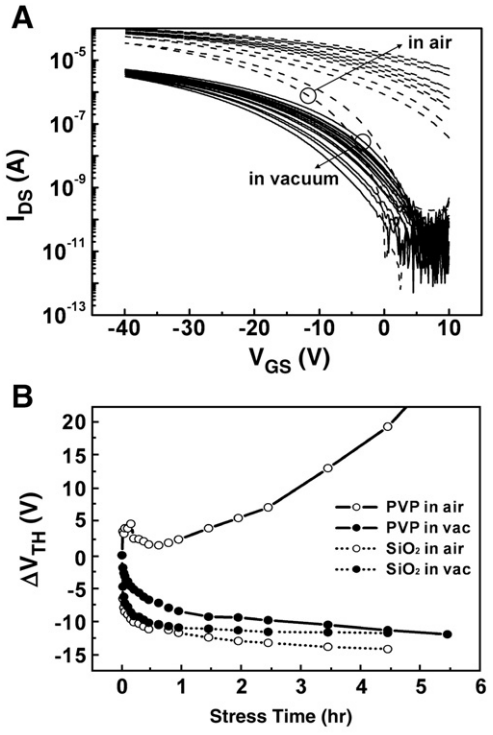

Fig. 1. A) Variation of transfer curves of pentacene TFTs using PVP gate dielectric under constant bias stress, B) Threshold voltage shift vs. stress time; for the PVP gate dielectric there was a negative shift when stressed in vacuum (a solid line with ●) while a positive shift occurred in air (a solid line with ○); for the SiO_2 gate, there was a negative shift in both vacuum (a dotted line with ●) and air (a dotted line with ○).

coated and cured at 200 °C according to a previously reported procedure [2], and the thickness was about 600 nm. Subsequently, pentacene with 60 nm thickness was evaporated through a shadow mask. Finally, the source and drain electrodes were formed by Au evaporation, resulting in top contact structure OTFTs. For comparison, we also fabricated pentacene TFTs using an SiO_2 gate in order to highlight the properties of the PVP gate. The channel length and width were 50 μm and 2000 μm, respectively.

A voltage of $V_{GS}=-20$ V to −5 V and $V_{DS}=-5$ V was applied to the OTFTS for the constant bias stress by semiconductor analyzer HP4155A from Hewlett–Packard for 6 h. The gate voltage stress was periodically stopped and the transfer curves were measured. The stress was carried out in vacuum as well as in air (25% humidity and 20 °C temperature) in order to elucidate the intrinsic properties from air effects. In addition, in order to identify a criterion to avoid the stress effects, we varied the gate stress voltage from −20 V to −5 V and analyzed the threshold voltage shift according to the gate voltages. Finally, we suggest a model for threshold voltage shift and a design rule to minimize the stress effects.

3. Results and discussions

As shown in Fig. 1A), the transfer curves varied with vastly different behavior depending on the environment. The shape changed considerably in air, implying severe degradation of mobility. The mobility degradation in air seems to be attributed to water vapors, which produce hydroxyl radicals in the pentacene grain boundaries [4]. This is supported by the finding that the mobility is stable in vacuum and even in air when OTFTs are protected from air via encapsulation, as noted in the literature [4].

Meanwhile, in vacuum the mobility was very stable as shown by the un-changed shapes of transfer curves. It exhibited the minor variation even after 6 h stress as shown in Fig. 2A). The mobility degradation was dependent on gate voltage, and especially enhanced above −15 V, exhibiting about 2% variation for $V_{GS}=-20$ V. The time variation of mobility was empirically formulated by Eq. (1)

$$\mu(t) = \mu_o e^{-\alpha t} \tag{1}$$

where α is the time constant of the mobility degradation and μ_o is the initial mobility. The α was extracted by comparing Eq. (1) with the mobility degradation graph of Fig. 2A), and plotted with respect to gate voltage as shown in Fig. 6A). The α exhibited a large increment above the gate stress voltage of −15 V. Therefore, the $V_{GS}=-15$ V seems to be a critical voltage for occurrence of stress effects. This issue will be discussed later in conjunction with threshold voltage shift.

The threshold voltage was shifted to the negative direction of gate voltage in vacuum whereas a positive shift occurred in air. In Fig. 1B), the threshold voltages of OTFTs with PVP and an SiO_2 gate are presented with respect to stress time. The OTFTs with an SiO_2 gate exhibited a negative shift of threshold voltage in vacuum as well as in air while the PVP gate produced a negative

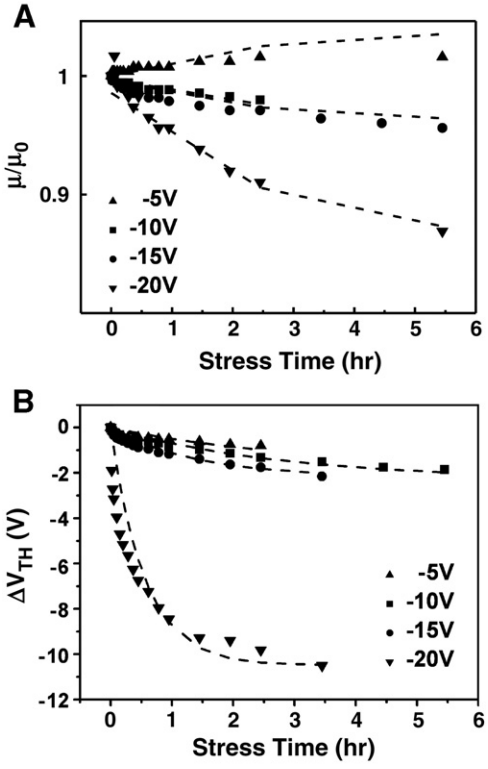

Fig. 2. A) The mobility variation vs. stress time, and B) the threshold voltage shift vs. stress time according to the applied gate stress voltage for PVP gate dielectric.