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ScienceDirect
Thin Solid Films 515 (2007) 6099–6102
www.elsevier.com/locate/tsf

# Strategies to increase CdTe solar-cell voltage

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Available online 15 December 2006

**Abstract**

There is a significant difference in performance between today's highest efficiency of CdTe solar cells and single-crystal cells of comparable band gap. The largest contribution to this difference is the voltage, where the values for the best CdTe cells are about 230 mV below the best GaAs cells when an appropriate adjustment is made for band gap. CdTe voltage and fill-factor are currently compromised by low recombination lifetime (near 1 ns), low hole density (near $10^{14}$ $cm^{-3}$), and in some cases an excessive back-contact barrier. Numerical simulation is used to evaluate how combinations of lifetime, carrier density, back electron reflection, and interfacial properties affect voltage and cell performance. Two different strategies for improving voltage and performance are explored.


*Keywords:* Solar cells; CdTe; Efficiency

## 1. Introduction

The record conversion efficiency of thin-film polycrystalline CdTe solar cells to date is 16.5% [1]. The open-circuit voltage of the highest efficiency CdTe cells, however, remains well below that of similar band-gap crystalline cells. This difference is illustrated in Fig. 1, where the current–voltage curve of the record-efficiency CdTe cell is overlaid with the curve derived from a high-efficiency GaAs cell [2]. A modest mathematical modification was done to adjust the GaAs band gap to that of CdTe, and hence the curve is labeled "GaAs". This adjustment increases the GaAs-cell voltage by 40 mV and decreases its current density by 1 $mA/cm^2$.

The salient feature of Fig. 1 is a 230-mV difference between the best CdTe cell and the adjusted "GaAs" cell. (There is also a modest current difference, but the current losses are well understood [3] and will not be discussed here). The analogous voltage difference for the other major thin-film polycrystalline solar cell, $Cu(In,Ga)Se_2$ (CIGS), is only about 30 mV when compared to crystalline silicon. If the CdTe voltage deficit were reduced to the same 30 mV, with the same current and fill-factor, CdTe cells would achieve 22% efficiency. The reason for the relatively low voltage of CdTe solar cells is a combination of low carrier density ($\sim 10^{14}$ $cm^{-3}$) and low absorber lifetime (generally below 1 ns). In some cases, the voltage is further compromised by the presence of a significant back-contact barrier.

## 2. Approach

This work employed numerical simulation to examine possible strategies for significantly reducing the CdTe voltage deficit. Both the AMPS [4] and SCAPS [5] software packages were utilized. Parameter values, unless otherwise stated, are the same as in Ref. [6]. Two distinctly different approaches for increasing voltage,

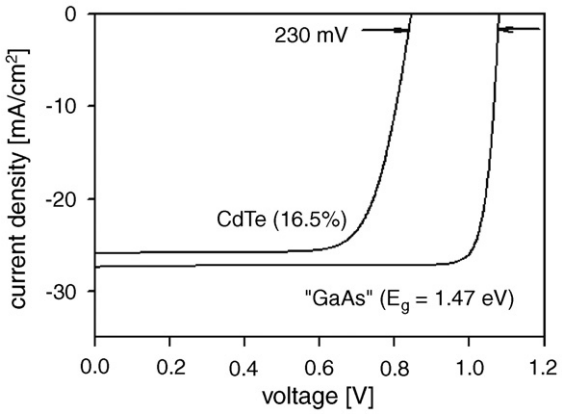


Fig. 1. Comparison of record CdTe cell with high-efficiency GaAs adjusted slightly for band gap.

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doi:10.1016/j.tsf.2006.12.147

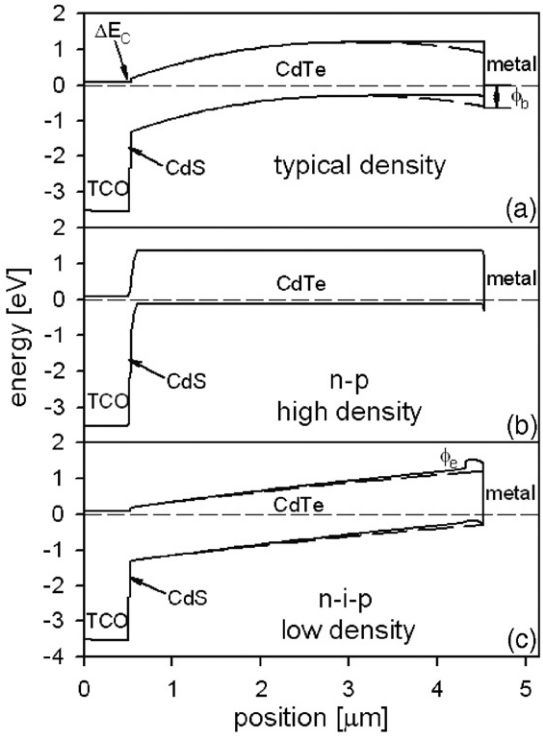


Fig. 2. (a) Band diagram of typical CdTe solar cell with and without a significant back-contact barrier. (b) Band diagram for significantly higher hole density. (c) Band diagram for lower density with and without an electron reflector.

which will be referred to as the "n–p" and the "n–i–p" strategies, were examined. Fig. 2a shows the band diagram of a CdTe solar cell with a thin n-CdS window layer. The low CdTe hole density ($2\times10^{14}$ cm$^{-3}$) in Fig. 2a is typical of today's cells and makes the CdTe absorber intermediate between i-type (intrinsic) and p-type. As a consequence, the depletion region extends over a large fraction, but not all, of the CdTe thickness. The possibility of a significant back-contact barrier $\phi_b$ is indicated by the dashed line. That possibility is evaluated in some detail in Ref. [7], but here the valence band will be assumed to be flat (the solid line in Fig. 2a) and not be further discussed.

Fig. 2b, where the hole density is increased to $2\times10^{17}$ cm$^{-3}$, is the classic n–p heterojunction. It is similar to what one would find with n-on-p GaAs, and we will explore what needs to be altered about the polycrystalline CdTe to achieve performance comparable to GaAs. In contrast, Fig. 2c lowers the hole density to $2\times10^{13}$ cm$^{-3}$, the CdTe becomes fully depleted, and the terminology used here is n(CdS)–i(CdTe)–p(back of CdTe). This configuration can also lead to high voltage, but of major importance in this case is the presence of an electron reflector $\phi_e$ at the rear on the absorber. As with the n–p configuration, the question for the n–i–p approach is what specifically needs to be done to achieve high voltage and efficiency.

A 4-μm CdTe thickness was used in all the simulations. Different thicknesses will alter the details, but in general not the form or the magnitude of the results. The transition from the "typical" band diagram (Fig. 2a) to the n–i–p structure (Fig. 2c), however, will occur at a different carrier density if the thickness is changed.

## 3. Results

### 3.1. Lifetime

Using the Fig. 2a band picture and hole density ($2\times10^{14}$ cm$^{-3}$), the current–voltage ($J$–$V$) curves were calculated as a function of the CdTe recombination lifetime $\tau$. Fig. 3a shows a series of $J$–$V$ curves for absorber lifetimes that span a range somewhat larger than the 0.2 to 2 ns typical of current cells. The "GaAs" curve is repeated for reference. Increasing carrier lifetimes leads to increased voltage and fill-factor. Physically, this would correspond to a smaller number of recombination defect states with the implicit assumption that the grain boundaries can be made benign. The large-$\tau$ fill-factor approaches that of GaAs and corresponds to a diode quality factor close to unity. The voltage, however, is limited by the separation of the quasi-Fermi levels and saturates at a value well below that of "GaAs", in fact only slightly above that which has been achieved experimentally. Hence, increasing lifetime alone

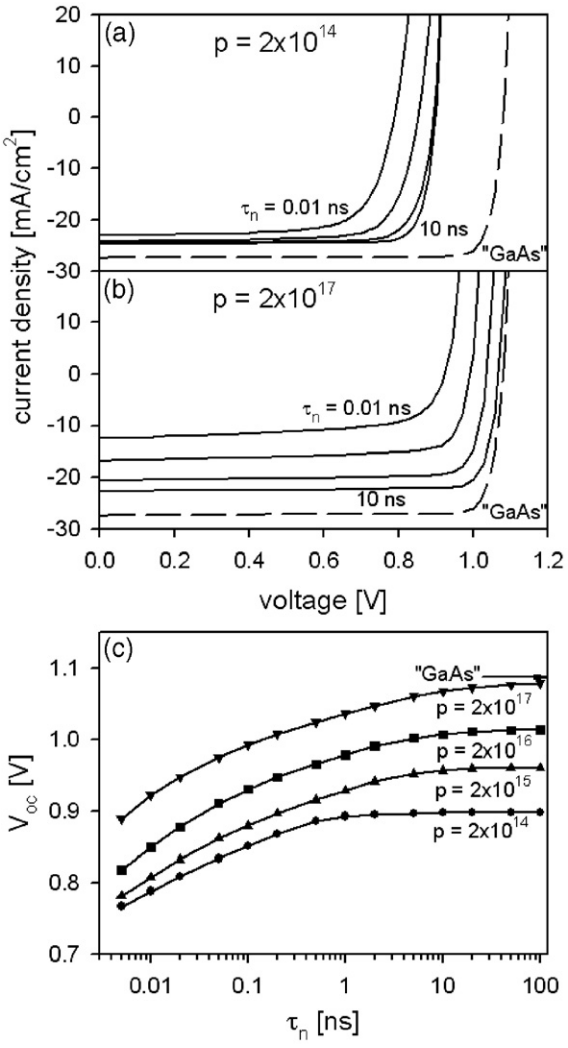


Fig. 3. (a) Simulated $J$–$V$ curves for typical-carrier-density CdTe with varying lifetime. (b) $J$–$V$ curves for high carrier density in same format. (c) Calculated voltage as a function of lifetime and carrier density.