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Expectation for Cat-CVD in ULSI technology and business trend

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Abstract

The ULSI technology has still been following Moor's Law in the sub-100 nm era, although several challenging issues must be solved in a practical environment. The first critical issue is, of course, how to make a sub-100 nm fine pattern. The second is to maintain the improvement of performance by lowering the RC delay, keeping a higher drivability of transistors, and suppressing the total chip power consumption as well as stand by power. The third issue is related to reliability and cost. Reliability relates to all other performance issues, but especially, high-k gate insulator integrity, interconnect reliability, thermal budget and process damage are major concerns. A discussion regarding the promising application of Cat-CVD (also called Hot-wire CVD) for solving these ULSI technology issues, such as low temperature, high-quality nitride film and hydrogen radical cleaning, is made in this paper.

Keywords: LSI; Cat-CVD; Silicon nitride; Ashing

1. Trend of ULSI technology

Fig. 1 shows the historical progress of the microprocessor in terms of the number of transistor integration, clock speed and manufacturing feature sire. Current typical numbers are more than l00 MTorr, 2–3 GHz, and 90 nm, respectively.

Fig. 2 shows an International Technology Roadmap for Semiconductors (ITRS) chart focusing on design rules of gate length. Depending on the device application in terms of power consumption, several design rules are used effectively. The actual scaling progress tends to be accelerated from the predicted timeline. Volume production of ULSI is now ongoing with 90 nm to 65 nm design rules, which incorporates 70 nm–30 nm level transistor gate lengths. The key parameters of CMOS 90 nm and 65 nm dimensions are summarized in Table 1. Gate insulator thickness must be shrunk to 1 nm Equivalent Oxide Thickness (EOT). It was shown in the recent IEDM [1–3] and VLSI symposium [4] that sub-10 nm gate transistors were fabricated with reasonable performance. Moor's Law will continue to this size level as long as device technology is concerned.

However, the fabrication lithography technology which is usable for less than 40 nm, is not yet clear. The wavelength of the light source has been getting shorter and from g-line to i-line to excimer KrF to ArF. FZ-Laser Lithography (157 nm) contains a lot of significant issues. EPL and Deep UV are alternative technologies [5] but will not be used as a real production tool at least for the next several years.

Fig. 3 summarizes current development items for 65 nm and beyond level of ULSI technology. The key is to introduce new materials of high-k and extreme low-k in the multilevel interconnect scheme.

Current ULSI, especially microprocessor and/or SoC devices, requires multi-level interconnects to 8–9 levels because of complexity and high circuit density. The RC delay of the circuit is a major performance issue today. Lower resistive material of Cu and low-k dielectric materials, such as SiOC and MSQ with a porous configuration instead of SiO_2 and FSG (SiOF), need to be applied in order to solve this issue. The trade off between low dielectric constant and mechanical strength for the CMP process is not yet solved. The latest data on the properties of these films are summarized in Table 2 [6]. The current dielectric constant target of the ILD material system is 2.5. Another issue is

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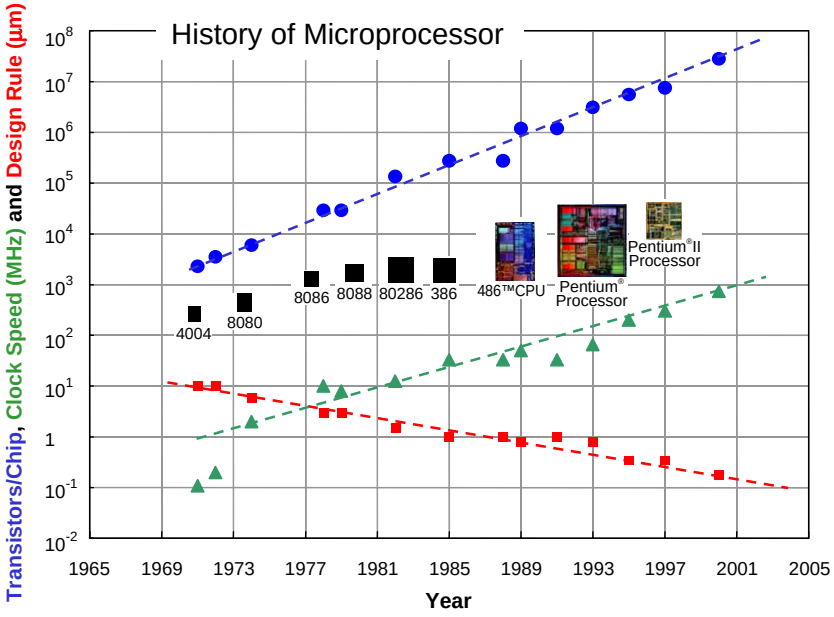

Fig. 1. Historical progress of LSI technology regarding microprocessor.

photo-resist removal or surface cleaning in this material system. A conventional oxygen plasma is known to provide serious oxidation damage to these materials, which results in the degradation of the dielectric constant itself.

A high-k gate is absolutely necessary for further scaling of transistors in order to keep higher current drivability as well as a permissible level of gate leakage depending on the system application. After a long and continuous research from various aspects, the tentative consensus is that HfSiO and/or HfAlO (or nitrized) are the most promising materials, which must replace the current SiN/SiO_2 system. Among several obstacles for the application of the high-k material, the most significant issues are mobility degradation, threshold voltage control and Negative Bias Temperature Instability (NBTI). A well-known approach to improve carrier mobility is to introduce stress in the channel region by forming an SiGe layer.

2. Expectation for Cat-CVD

For a high performance transistor, a lower thermal budget is strongly required. Cat-CVD is a potential candidate to replace some of conventional film deposition technologies because of its lower temperature process capabilities. Table

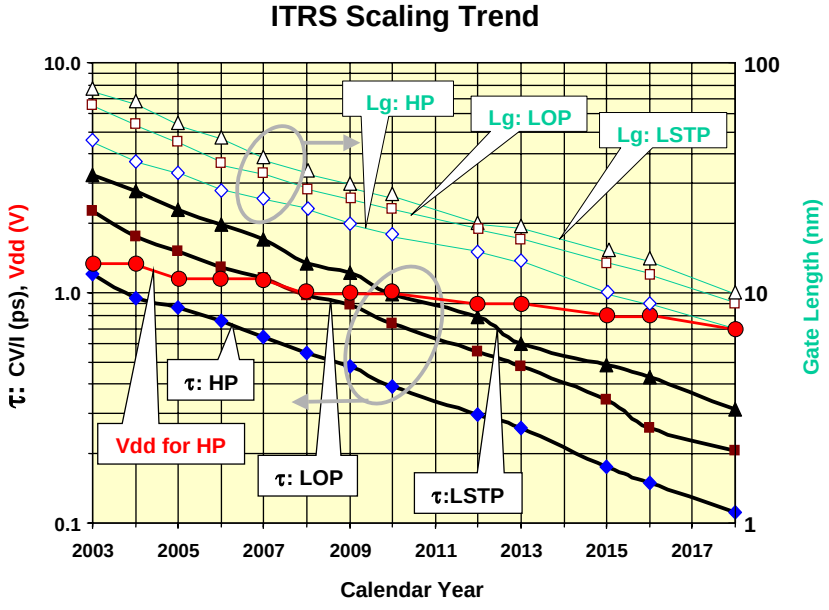

Fig. 2. Trend of gate insulator thickness and gate speed (by ITRS).