

# Effect of emitter deposition temperature on surface passivation in hot-wire chemical vapor deposited silicon heterojunction solar cells

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## Abstract

Low substrate temperature ( $<150\text{ }^{\circ}\text{C}$ ) during initiation of amorphous silicon emitter deposition by hot-wire chemical vapor deposition is found to be crucial for reaching high open-circuit voltage ( $V_{oc}$ ) in an amorphous/crystalline silicon (a-Si/c-Si) heterojunction solar cell. Low-temperature results in immediate a-Si deposition and a smooth interface to the c-Si substrate. The smooth heterojunction leads to effective passivation of the c-Si surface by the a-Si intrinsic layer through a much-reduced interface recombination velocity, and  $V_{oc}$  is consistently above 620 mV. We obtain a  $V_{oc}$  above 640 mV and a fill factor of 80% on Al-backed p-type Czochralski wafers with emitters deposited at temperatures below  $135\text{ }^{\circ}\text{C}$ . Energy conversion efficiencies of 14.8% and 15.7% are obtained on a polished p-type Czochralski silicon wafer and a polished p-type float-zone silicon wafer, respectively.

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## 1. Introduction

Hot-wire chemical vapor deposition (HWCVD or Cat-CVD) may ultimately be superior to plasma-enhanced CVD (PECVD) for silicon heterojunction solar cells because 1) ion bombardment damage to the crystalline Si (c-Si) wafer is avoided, 2) atomic hydrogen (H) can easily be generated to pre-clean and passivate the wafer, and 3) powder formation which might short the thin hydrogenated amorphous silicon (a-Si:H) emitter layers is unlikely. However, high performance silicon heterojunction solar cell emitters have thus far been deposited only by PECVD [1,2].  $V_{oc}$  is usually well below 600 mV when HWCVD emitters are deposited on p-type Czochralski (CZ-Si) wafers [3].

Under many conditions, HWCVD results in low-temperature epitaxy of silicon on c-Si substrates [4] at temperatures as low as  $195\text{ }^{\circ}\text{C}$ . In high-efficiency heterojunction solar cells, a thin ( $\sim 5\text{ nm}$ ) intrinsic a-Si:H layer must be interposed between the base wafer and the heavily doped a-Si:H emitter [5], because intrinsic a-Si:H has a far lower density of

defects than a doped a-Si:H layer [6]. A lower density of mid-gap trap states reduces the trap-assisted inter-band tunneling-recombination rate across the a-Si/c-Si interface, thereby suppressing deleterious saturation current. On the other hand, if there is unintentional Si epitaxy rather than a-Si:H deposition, the epitaxy may be defective and the interface rough, resulting in unpassivated silicon dangling bonds or other defects. Worse, if epitaxy extends through the i-layer and c-Si contacts the doped a-Si:H, enhanced recombination will result. Thus, if epitaxial growth is avoided when we deposit the intrinsic/doped a-Si emitter, we maintain a minimum interface area, and reduce both the Shockley–Read–Hall recombination in the space-charge region and the trap-assisted tunnelling recombination across the interface. A well-passivated heterojunction results in high performance HWCVD silicon heterojunction solar cells with high open-circuit voltage and fill factor.

## 2. Experimental

Detailed description of substrates, cleaning procedure, and device structures are reported elsewhere [7], although

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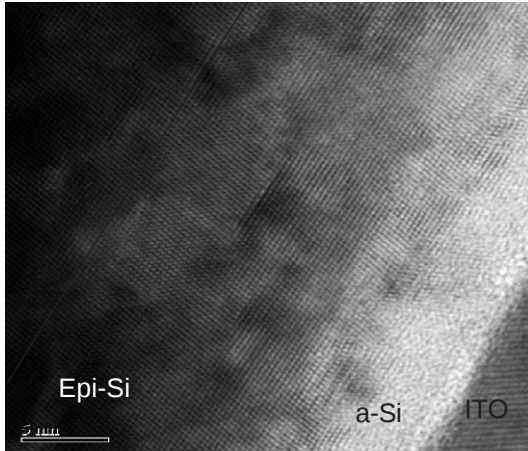


Fig. 1. HRTEM image of Si emitter deposited on a (111) wafer at 375 °C. Line shows the wafer surface.

in that reference we reported the temperature of the substrate canister. In this paper, we report the actual substrate temperature during deposition, accurate to  $\pm 20$  °C. We use tungsten- or tantalum-wire HWCVD to deposit intrinsic and phosphorous-doped a-Si:H layers (i- and n-layer) on p-type c-Si wafers that have an alloyed aluminum back-surface-field (Al-BSF). The deposition chamber is equipped with optical access ports for real-time spectroscopic ellipsometry (RTSE) at a 70° angle of incidence. Using RTSE [8] feedback for thickness control, a 5- to 10-nm intrinsic a-Si:H layer is grown using 20 sccm of SiH<sub>4</sub> at 10 mTorr, followed by a 15-nm n-layer by using 2.5 sccm of SiH<sub>4</sub>, 3 sccm of 5% PH<sub>3</sub> in H<sub>2</sub>, and 50 sccm of H<sub>2</sub> at 60 mTorr. Post-deposition analysis of RTSE data [7] and cross-sectional high-resolution transmission electron microscopy (HRTEM) are used to detect even a few monolayers of epitaxial growth in emitter deposition.

The most direct way of evaluating the quality of an emitter is to finish the solar cell with a transparent conductor, grid and mesa etch, and to measure its illuminated electrical performance, especially  $V_{oc}$ . A more expedient way of characterizing an a-Si/c-Si heterojunction is to measure the interface recombination velocity  $S$ , because the diode saturation current  $J_{oe}$  (which in turn determines  $V_{oc}$ ) under the solar cell operation condition is related to  $S$  via [9]  $J_{oe} = \frac{qS\bar{n}_i^2}{\bar{n}}$ , where  $\bar{n}$  is the photo-carrier density and  $n_i$  the intrinsic carrier density in c-Si.  $S$  can be easily evaluated by effective lifetime measurement from photoconductivity decay (PCD) [10], using a symmetric a-Si/c-Si/a-Si “sandwich” structure:

$$\frac{1}{\tau_e} = \frac{1}{\tau_b} + \frac{2S}{W}$$

where  $\tau_e$  is the measured photoconductivity decay time,  $\tau_b$  is the true bulk lifetime due to Shockley–Read–Hall and Auger recombinations, and  $W$  is the c-Si wafer thickness. It is apparent that a low  $S$  value is essential for an emitter

to be effective in achieving a low saturation current and high  $V_{oc}$ .

### 3. Results and discussions

Our most striking result is that when there is epitaxy in the emitter,  $V_{oc}$  can barely exceed 600 mV; the exact value depends on how defective the epitaxy is and how rough the a-Si/c-Si interface is. The tendency to grow epitaxial c-Si in the emitter is found to be very sensitive to the crystal orientation of the substrate. RTSE clearly indicates epitaxial growth up to 30 nm in thickness on a (100) substrate at 200 °C. On a (111) substrate at the same temperature, however, RTSE showed the film to be essentially a-Si:H as soon as the deposition starts.

When the substrate temperature is higher, epitaxial growth can also be observed on (111) substrates. The HRTEM image of Fig. 1 shows that epitaxy persists for  $\sim 15$  nm at 375 °C on a (111) wafer, extending through the 5-nm i-layer and well into the n-layer. As a result, the  $V_{oc}$  of this device is only 487 mV. However, Fig. 2 shows that when we lower the substrate temperature to 100 °C for both the i- and n-layer deposition, abrupt amorphous silicon growth is obtained, even on a (100) wafer. A  $V_{oc}$  of 628 mV is obtained on this device.

Because of the tendency to deposit a-Si:H at lower substrate temperatures,  $V_{oc}$  increases with decreasing emitter deposition temperature. This increase of  $V_{oc}$  is directly linked to the reduction in dark current. Fig. 3 shows plots of dark current (uncorrected for the effect of series resistance at high current) for several i- and n-layer deposition temperatures (same for both layers) for 0.4  $\Omega\cdot\text{cm}$  (111) substrates. The diamonds, triangles, and rectangles represent diode dark currents for deposition temperatures of 375, 200, and 100 °C, respectively. For reference, the solid line shows the dark current for a diffused junction fabricated on a similar substrate with an

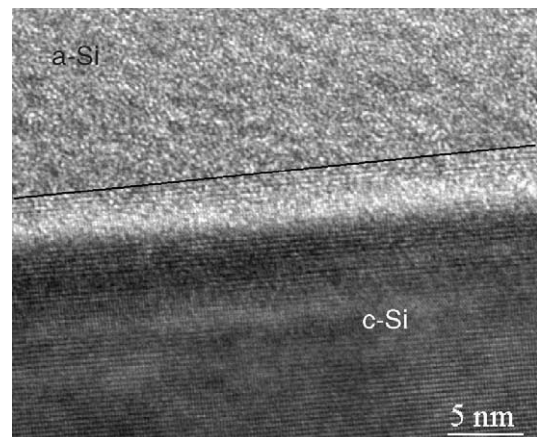


Fig. 2. HRTEM image of Si emitter deposited on a (100) wafer at 100 °C. Line shows the wafer surface.

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