Ultramicroscopy 170 (2016) 69–76

Contents lists available at ScienceDirect

Ultramicroscopy

journal homepage: www.elsevier.com/locate/ultramic

High temperature conductance mapping for correlation of electrical properties with micron-sized chemical and microstructural features

Karin Vels Hansen [a,*], Kion Norrman [a], Torben Jacobsen [b]

[a] Department of Energy Conversion and Storage, Technical University of Denmark, Frederiksborgvej 399, DK-4000 Roskilde, Denmark
[b] Department of Chemistry, Technical University of Denmark, Kemitorvet Building 207, DK-2800 Lyngby, Denmark

ARTICLE INFO

Article history:
Received 25 March 2016
Received in revised form
11 July 2016
Accepted 25 July 2016
Available online 18 August 2016

Keywords:
High temperature scanning probe microscopy
In situ scanning probe microscopy
Conductance
Microelectrodes
Secondary phases

ABSTRACT

High temperature AC conductance mapping is a scanning probe technique for resolving local electrical properties in microscopic areas. It is especially suited for detecting poorly conducting phases and for ionically conducting materials such as those used in solid oxide electrochemical cells. Secondary silicate phases formed at the edge of lanthanum strontium manganite microelectrodes are used as an example for correlation of chemical, microstructural and electrical properties with a spatial resolution of 1–2 μm to demonstrate the technique. The measurements are performed in situ in a controlled atmosphere high temperature scanning probe microscope at 650 °C in air.

1. Introduction

In situ and in operando techniques are increasing in number due to the need for assessing properties of functional materials while they are at work as compared to ex situ analyses where the conditions may deviate so much that it influences the properties to be determined. Many properties of solid oxide cell (SOC) materials cannot be investigated at room temperature due the temperature dependence of conductivity of the electrolyte and the electrocatalytic properties of the electrodes. Detailed investigation of degradation mechanisms of SOCs are difficult to perform in operando as the vital locations are inaccessible, and further, SOC electrodes have complicated three dimensional microstructures which are difficult to describe and quantify as they have a porous microstructure and consist of two or more phases. The triple phase boundaries (TPB) where the gas, electrode and electrolyte meet and where the electrochemical reactions take place are not visible or accessible and the TPB properties cannot easily be evaluated. Local measurements of the TPB may be performed in model systems such as microelectrodes where the simple geometry makes the accessibility easy and the calculation of parameters such as TPB length and surface and interface areas uncomplicated.

With scanning probe microscopy (SPM) such as a controlled atmosphere high temperature scanning probe microscope (CAHT-SPM) [1] microelectrodes and their TPB can be addressed individually, and local electrical or electrochemical properties can be measured in situ or in operando. The CAHT-SPM was developed to study electrical properties of high temperature materials in controlled atmospheres and works in the temperature range of 25–850 °C and with in-house fabricated Pt-10% Ir probes [2] which have good mechanical properties also at high temperature.

Electrical measurements used in scanning probe microscopy are abundant and comprise e.g. scanning tunneling microscopy and spectroscopy, Kelvin probe microscopy, conductive atomic force microscopy but also other techniques for measuring impedance, capacitance, resistance etc. have been reported [3]. The majority of literature on SPM concerns measurements at temperatures below ~200 °C and measurements at higher temperatures combined with a controlled atmosphere at atmospheric pressure are very limited, as recently reviewed by Nonnenmann [4]. With the CAHT-SPM we have developed a technique based on AC conductance measurements using a lock-in amplifier. This technique is ideal for conducting materials with relatively low conductances or poorly conducting phases. Conductance maps can be acquired quickly and simultaneously with topography images [1] and small inhomogeneities with a lateral extension of 1–2 μm can be revealed.

The present report explains the main principles of the conductance mapping technique and demonstrates how micron-sized features in the conductance images correlate well with features recorded by time-of-flight secondary ion mass spectrometry (TOF-SIMS) imaging and microstructural features observed in scanning

* Corresponding author.
E-mail address: karv@dtu.dk (K.V. Hansen).

http://dx.doi.org/10.1016/j.ultramic.2016.07.019
0304-3991/

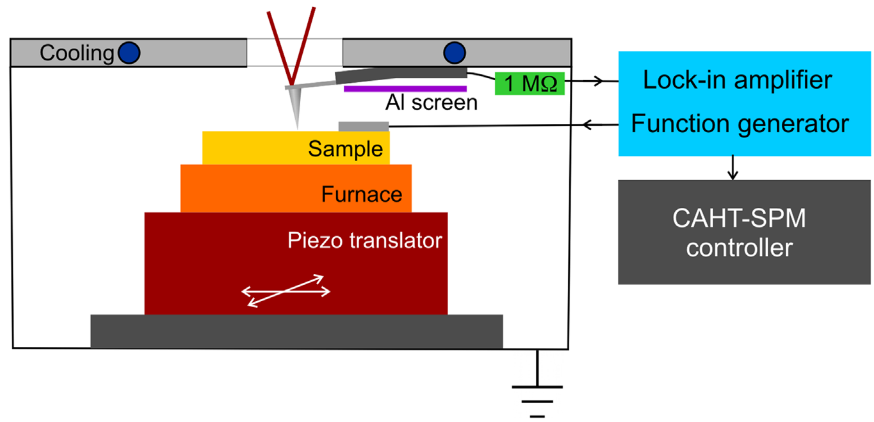

Fig. 1. The set-up in the CAHT-SPM during conductance mapping. The aluminum screen (purple) minimizes stray capacitance between cantilever and sample.

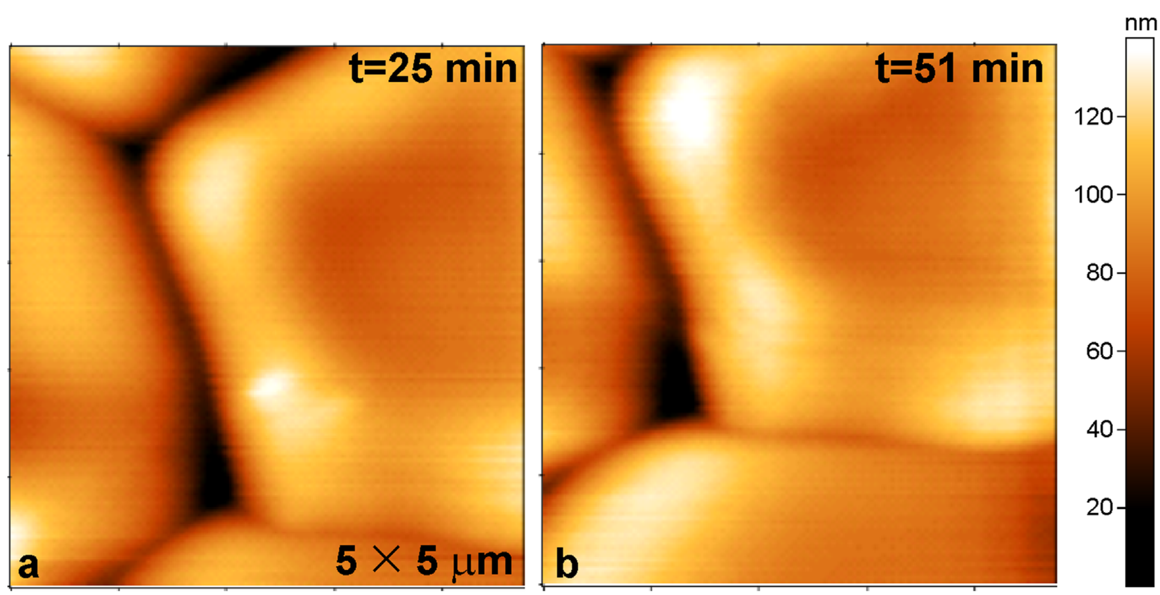

Fig. 2. Drift study of polished and heat treated zirconia with an in-house made Pt/Ir probe. The sample temperature is 600 °C, the scan speed is 5 µm/s. Time, *t*, is counted from when the sample reached 600 °C. Over 26 min the drift is less than 1 µm in both the x- and y-direction.

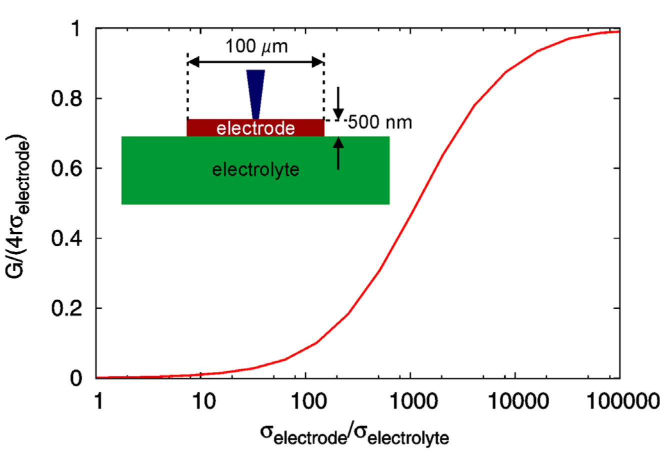

Fig. 3. Conductance measured with the probe in the center of a circular thin-film microelectrode deposited on a substrate as function of the conductivity of the electrode material relative to that of the substrate. The conductance is normalized with the value corresponding to an infinite ratio. The graph is the result of finite element calculations using the FreeFem++ program [13].

electron microscopy (SEM) images thus validating the observations in the CAHT-SPM.

Previously, lanthanum strontium manganite (LSM) microelectrodes on yttria-stabilized zirconia (YSZ) were characterized by impedance spectroscopy and cyclic voltammetry in a CAHT-SPM [5], microstructurally by SEM [5] and chemically by TOF-SIMS [6]. Here they are used as an example to demonstrate the correlation between electrical, chemical and microstructural properties.

2. Materials and methods

2.1. Conductance mapping

The sample is mounted on the furnace of the CAHT-SPM (Fig. 1) and kept in place by springs pressing the sample against the furnace. A platinum wire counter electrode is attached to the edge of the sample. A sine wave AC voltage is applied to the tip or the sample by the sine wave generator of a Stanford SR830 lock-in amplifier. The resulting current is measured by the lock-in amplifier through a 1 MΩ resistor for overload protection to avoid overload on samples with highly conducting regions. The current output of the lock-in amplifier is then directed to the external input option of the CAHT-SPM controller and depicted along with the topography during normal contact mode scanning. The conductance, $G = 1/(R + 1\ \mathrm{M\Omega})$ where R is the local sample resistance