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In situ measurements and transmission electron microscopy of carbon nanotube field-effect transistors

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Abstract

We present the design and operation of a transmission electron microscopy (TEM)-compatible carbon nanotube (CNT) field-effect transistor (FET). The device is configured with microfabricated slits, which allows direct observation of CNTs in a FET using TEM and measurement of electrical transport while inside the TEM. As demonstrations of the device architecture, two examples are presented. The first example is an *in situ* electrical transport measurement of a bundle of carbon nanotubes. The second example is a study of electron beam radiation effect on CNT bundles using a 200 keV electron beam. *In situ* electrical transport measurement during the beam irradiation shows a signature of wall- or tube-breakdown. Stepwise current drops were observed when a high intensity electron beam was used to cut individual CNT bundles in a device with multiple bundles.

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1. Introduction

The discovery of carbon nanotubes (CNTs) by Iijima [1] have attracted considerable interest and research into their electric transport properties, especially single-walled carbon nanotubes (SWNTs). While the structure and properties of a SWNT can be predicted by theory [2], multi-walled carbon nanotubes (MWNTs) or SWNT bundles are much more complicated and little understood due to the combinations of individual metallic and semiconducting tubes, tube–tube interactions, and tube configurations with respect to external fields [3,4]. Recently, several groups have determined the structure of different forms of CNTs using electron diffraction (ED) [5–8]. However, most of the structure determinations were performed separately without electrical transport measurement. In a few cases reported, electric measurements were done using two probes [9–11].

A CNT field-effect transistor (CNTFET) fabricated using chemical vapor deposition (CVD) is one of the commonly used approaches to study electrical transport in CNTs [12,13]. However, due to the self-assembly process of the CVD growth, a mixture of CNTs of different forms is often produced, which, in turn, yields device characteristics that are difficult to interpret without the knowledge of the CNT structure. The commonly used geometry of an FET device is not suited for transmission electron microscopy (TEM) characterization of CNTs. Chikkannanavar et al. [14], Meyer et al. [15], and Obergfell et al. [16] have presented electronic devices which are compatible with TEM study. Their devices were fabricated by the deposition of metal electrodes on top of CVD-grown CNTs suspended across pre-defined holes in silicon nitride membranes [14] or at edges created by cleaving and etching the Si wafer on which the device was built [15,16]. We have also reported a device architecture for electrical transport measurement and TEM observation [17]. However, *ex situ*

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electrical measurements were performed for device characterization.

Here, we report a modified design and fabrication of an array of CNTFETs with slits etched through the substrate and their integration with a custom-built electrical holder for *in situ* TEM measurements [18]. The main advantage of *in situ* measurement is that electrical transport properties of CNTs can be directly interpreted in conjunction with the structure, and electron radiation can be combined with transport measurements to allow a study of defects on CNT transport properties. The *in situ* microscopy methods reported here can also be used for studying other one-dimensional nanostructures.

2. Experiments—sample preparation and experimental setups for *in situ* TEM

The dimension of the sample is $5 \times 10\,mm^2$ with 7 rows $\times$ 14 columns of FET devices fabricated in one sample. The fabrication starts with a highly doped, p-type, 4-in. silicon-on-insulator (SOI) wafer with a 10-μm-thick Si device layer on top of a 2-μm-thick buried oxide (BOX) layer. Arrays of $100 \times 100\,\mu m$ windows are etched on the back side of the SOI wafer which stops at the Si device layer. This is then followed by creation of a 2–3 μm width 100 μm long slits etched on the front device layer. After etching the slits, a 250 nm thick of SiO_2 film was thermally grown at 1100 °C. The details of the fabrication are described elsewhere [17]. There are two main differences between the previous report and the device fabrication described here: (1) the CNTs here are grown using an ultra thin metal film catalyst [19] and (2) electrodes are defined after CNT growth. The metal catalyst layer used here is Fe/Al of 1.0/8.0 nm thick, respectively. The film is deposited using an electron-beam evaporator under a slow deposition rate (0.1 Å/s or lower). The growth temperature is 900 °C and carbon feedstock is ethanol (C_2H_5OH) vapor with a mixture of H_2 and Ar. The thin metal film catalysts on an oxide surface give better control over the number of tubes bridging the slits than wet-solution catalyst. After CNT growth, optical lithography, metal deposition (Au/Ti, 5/30 nm, respectively), and the lift-off process are followed to form the electrodes. Before the metal deposition, SiO_2 at the corner of the sample is etched for gate formation. The gate electrode is patterned directly onto the highly doped (0.005–0.02 Ω cm) device layer.

Fig. 1(a) shows a device array. All the drain electrodes are connected together due to the geometry of the TEM holder (see Fig. 2(a)). Fig. 1(b) shows a fabricated device with a small carbon nanotube bundle across the slit. The inset illustrates a schematic diagram of the device in the cross-section view. The devices selected from scanning electron microscopy (SEM) characterization [17] are connected to source electrode bridges using dual beam focused ion beam (FIB). Fifty-nanometer-thick Pt is deposited with the help of a Ga ion source. Figs. 1(c) and (d) show a selected device before and after Pt deposition (see the solid-lined boxes). The sample is then mounted on the custom-made specimen holder for a JEOL 2010F. Figs. 2(a) and (b) show the holder without and with the sample mounted. There are eight electrodes which can be connected to the outside control instrument. In our device geometry, two common electrodes for gate and drain are permanently used and four electrodes are contacted to the

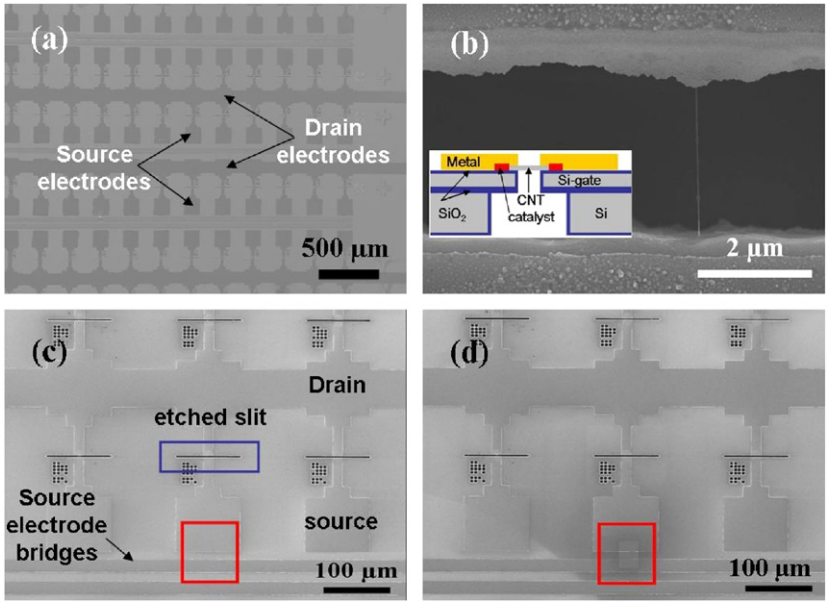

Fig. 1. (a) Scanning electron micrograph of the device arrays. All the drain and gate electrodes are common. Source electrode bridges are used for interconnection of individual devices with electrical pads for measurements. (b) SEM image of a CNT bundle connecting source and drain across the slit. The inset illustrates a schematic diagram of the device. Images of individual device (c) before and (d) after the interconnection by FIB are shown (boxed area).