Ultramicroscopy 108 (2008) 1045–1049

Contents lists available at ScienceDirect

Ultramicroscopy

journal homepage: www.elsevier.com/locate/ultramic

Local inhomogeneity in gate hysteresis of carbon nanotube field-effect transistors investigated by scanning gate microscopy

Joon Sung Lee [a,b], Sunmin Ryu [a], Kwonjae Yoo [a], Jinhee Kim [a], Insung S. Choi [b,1], Wan Soo Yun [a,*]

[a] Division of Advanced Technology, Korea Research Institute of Standards and Science, Daejeon 305-600, Republic of Korea
[b] Department of Chemistry and School of Molecular Science (BK21), KAIST, Daejeon 305-701, Republic of Korea

ARTICLE INFO

PACS:
85.35.Kt
87.64.Dz
84.37.+q
68.47.Gh

Keywords:
SGM
CNFET
CNT
Charge trap
Defect
Silicon oxide

ABSTRACT

Local nature of gate hysteresis in a carbon nanotube field-effect transistor (CNFET) was studied using scanning gate microscopy (SGM). A sequential set of SGM images of the CNFET fabricated on a SiO_2/Si substrate was obtained at a low temperature under an ultra-high vacuum. Comparisons of the SGM images obtained at decreasing and increasing gate voltage steps revealed that the order of appearance of SGM defects could not be accounted for by a uniform distribution of hysteretic gate screening along the carbon nanotube (CNT) channel. It was concluded that the gate hysteresis in the CNFET had substantial local variations along the CNT. The local inhomogeneity in gate hysteresis was attributed to inhomogeneous distribution of screening charge traps or sources on the SiO_2 surface.

1. Introduction

Scanning gate microscopy (SGM) has been one of the most effective methods for local characterization of nanoscale electronic devices. In SGM, a scanning probe is used as a moving gate electrode which locally modulates gating field applied to the measured device [1]. As electric conductance of the device is recorded as a function of the probe position, variations in susceptibility of the device to the gating field can be spatially resolved. This method has been successfully utilized to reveal essential characteristics in various nanoscale electron transport systems. For example, it has been discovered by SGM that carbon nanotube field-effect transistors (CNFETs) often have some 'defects' that can act as bottlenecks to current transport near the on–off transition region [2,3].

Since its introduction as a prominent candidate for future-generation electronic device [4], CNFET has been one of the most intensively studied systems in the field of nanoscale electronic devices. Its potential applications range widely from universal electronic transistors to biosensors. However, there are several issues which inhibit practical implementation of CNFETs, such as device integration and property control of the carbon nanotubes (CNTs). Gate hysteresis is another important issue in the field of research on CNFETs.

Gate hysteresis in CNFET is a phenomenon in which transfer characteristics of a CNFET are not determined uniquely by gate voltage values but affected by history of applied gate voltages. This phenomenon is known to be caused by trapped screening charges near the CNT, which are generated by electric fields between the gate electrode and the CNT [5,6]. It is also known that gate hysteresis is largely affected by adsorbed gas molecules such as water [7]. We have previously shown that the screening charges that cause gate hysteresis in CNFETs on SiO_2 substrates are confined to the device surfaces, and proposed surface silanol groups as sources of the screening charges [8].

Although gate hysteresis in CNFETs has been investigated by a number of works [5–9], studies on spatially resolved characteristics of gate hysteresis have been very scarce. Staii et al. [10] have reported tip gate-induced hysteresis ('memory effect') in a CNFET. In their work, hysteretic local gate responses were found only near SGM defects in the CNFET. Here, the term 'SGM defects' was used to represent locations along the CNT where significant local conductance modulations could be observed in SGM. Hence, it was natural that hysteretic responses were not observed where conductance modulations by tip gating were nonexistent, as was pointed out by the authors as well. Therefore, the above report could give no further clue as to the local nature of gate hysteresis.

As investigations on local characteristics of gate hysteresis still remain desirable, we performed SGM on a CNFET at 102 K under

* Corresponding author. Tel.: +82 42 868 5952; fax: +82 42 868 5953.
E-mail addresses: ischoi@kaist.ac.kr (I.S. Choi), wsyun@kriss.re.kr (W.S. Yun).
[1] Tel.: +82 42 869 2840; fax: +82 42 869 2810.

0304-3991/$ - see front matter © 2008 Elsevier B.V. All rights reserved.
doi:10.1016/j.ultramic.2008.04.067

an ultra-high vacuum (UHV), which clearly revealed the local nature of gate hysteresis in CNFETs. In this work, observed SGM defects were used as watermarks for local electrostatic potential profile near the CNT [3]. From comparisons between SGM images acquired at sequential gate voltage steps, we found that gate hysteresis in the CNFET had a locally inhomogeneous character. Since gate hysteresis in a CNFET is caused by gate-screening surface charges trapped nearby, the local inhomogeneity in gate hysteresis could be attributed to an inhomogeneous distribution of screening charge traps or sources on the silicon oxide substrate.

2. Experimental

The CNFET used in this work was fabricated on a degenerately *p*-doped silicon substrate covered with a 550 nm-thick thermally grown oxide layer. Au contact pads and catalyst islands were defined on the substrate by photolithography and e-beam lithography. Single-walled carbon nanotubes (SWCNTs) were directly grown from the catalyst islands by chemical vapor deposition [11]. After a grid pattern was formed on the sample by e-beam lithography, individual CNTs were located using an atomic force microscope (AFM) with respect to the predefined Au grid pattern. Source and drain contacts were formed on a SWCNT as thermally evaporated 10 nm-thick Pd layers defined by e-beam lithography. The channel length of the device was 4 μm, and the diameter of the CNT was measured to be about 2 nm. The band gap of the SWCNT was determined to be $\geqslant 0.4$ eV from a conductance–drain voltage–gate voltage (G–V_{ds}–V_g) measurement over the semiconducting gap region at 50 K. This value roughly agreed with the measured diameter of the CNT [12], thus eliminating the possibility of a bundled CNT.

Measurements were made by using an Omicron UHV–VT–AFM which had been modified to enable *in-situ* electron-transport measurements on device samples mounted on the SPM stage. With the SPM system (base pressure $\approx 1\times10^{-10}$ mbar), it was possible to measure electrical conductance of a device simultaneously with SPM scans within a temperature range of 50–297 K. The sample temperature was determined by a calibration equation obtained from an independent cooling test of a similarly constructed dummy sample installed on the SPM stage. During the cooling test for calibration, temperature of the dummy sample was obtained by four-probe measurements of a Pt resistance-temperature sensor (Lakeshore Pt-111) fixed on the sample, and recorded along with temperature readings from two built-in temperature sensors. A temperature calibration equation was devised to approximate the sample temperature from the built-in temperature sensors' readings. It was also possible to anneal device samples at temperatures over 300 °C in the UHV system. The CNFET sample was thermally annealed at 200 °C for 3 h to remove possible residual gas molecules such as water adsorbed on the sample surface.

Device topography in this work was obtained in frequency-modulated noncontact mode [13]. During SGM measurements (Fig. 1), dc source current of the CNFET (with $V_d = 10$ mV and $V_s = 0$ V) was measured by using a current–voltage amplifier (DL Instruments model 1211) and recorded as a function of position of the tip scanned with a constant tip height of 200 nm. The scan speed (1.5 μm/s) and scan-initializing conditions were maintained throughout the experiment to avoid possible errors from creep in the piezoelectric scanner. The back-gate voltage (V_g) applied to the sample was changed in arbitrary steps, but the range and direction of the steps were kept the same with the subsequent current–gate voltage (I–V_g) measurement ($V_g = +20 \rightarrow -20 \rightarrow +20$ V).

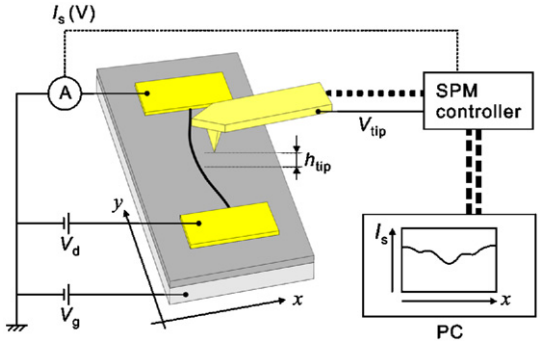

Fig. 1. Measurement scheme for the SGM experiment. Source current (I_s) of the CNFET driven by a drain voltage (V_d) of 10 mV was measured as a function of position of the scanned tip which worked as a moving secondary gate electrode. Tip–sample distance (h_{tip}) was kept at ~200 nm, and sample temperature was kept at ~102 K. The measurements were done under a UHV.

3. Results and discussion

When measured in air, the CNFET exhibited a *p*-channel-dominant ambipolar character with a large advancing gate hysteresis. After a thermal annealing at 200 °C for 3 h under UHV, the device changed to an *n*-channel-dominant ambipolar CNFET. Such a change in device character had been explained by a change of Fermi-level alignment at the CNT-metal contacts due to desorption of gas adsorbates such as oxygen from the electrode surfaces [14]. However, the gate hysteresis could still be observed after the thermal annealing and cooldown to 50 K, although it decreased quite a bit [5].

After the sample temperature was settled at 102 K, the device topography was obtained with a Pt-coated AFM probe in non-contact mode. Fig. 2a is a frequency-shift (Δf) image of the CNFET obtained at $V_g = 0$ V after several V_g sweeps. In this image, some irregularly shaped low bumps could be seen near the CNT. They did not represent the real topography, but were generated by increased tip–sample electrostatic forces due to static charges built up near the CNT by previous gate sweeps, for these bumps could be suppressed by using larger Δf setpoints or by applying adequate tip biases. It was found that such static charges could be dissipated by brief thermal annealing at 150 °C, and then could be regenerated by gate voltage sweeps. Obviously, these static charges are remainder of the trapped gate-screening charges that are responsible for the gate hysteresis [8].

Afterward, we performed SGM in the same scan range. The SGM images (Figs. 2c–j) were characterized by many concentric ring patterns centered along the CNT. Such SGM patterns, frequently observed in long-channel CNT devices at low temperatures, have been attributed to Coulomb oscillations from quantum dots (QDs) formed in the CNTs by local potential corrugations near the CNTs [15,16]. During SGM scans on such a CNT device, the biased tip, which sweeps over QDs in the CNT, will modulate electrostatic potential of the QDs according to the distances from them. The potential modulation on each QD will cause Coulomb oscillations, of which the sum should be expressed as an SGM image characterized by concentric ring patterns centered on the QDs. However, because tunnel barriers that form such QDs are not definite but prone to the tip gating, the resultant conductance oscillations may not be regular as expected for well-defined QDs.

The local potential corrugations that may form such QDs in a semiconducting CNT can be compensated for with sufficiently many charge carriers when the Fermi level of the CNT is placed well above the conduction band edge or well below the valence band edge of the locally corrugated band structure [16]. In other words, a QD formed by local potential corrugations will be