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Tungsten contamination in ion implantation

M.L. Polignano *, F. Barbarossa, A. Galbiati, D. Magni, I. Mica

STMicroelectronics, Via Olivetti, 2, 20864 Agrate Brianza (MB), Italy

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ABSTRACT

In this paper the tungsten contamination in ion implantation processes is studied by DLTS analysis both in typical operating conditions and after contamination of the implanter by implantation of wafers with an exposed tungsten layer. Of course the contaminant concentration is orders of magnitude higher after contamination of the implanter, but in addition our data show that different mechanisms are active in a not contaminated and in a contaminated implanter. A moderate tungsten contamination is observed also in a not contaminated implanter, however in that case contamination is completely not energetic and can be effectively screened by a very thin oxide. On the contrary, the contamination due to an implantation in a previously contaminated implanter is reduced but not suppressed even by a relatively thick screen oxide. The comparison with SRIM calculations confirms that the observed deep penetration of the contaminant cannot be explained by a plain sputtering mechanism.

1. Introduction

Sputtering is a very common contamination mechanism in ion implantation [1], because material sputtered by the ion beam from parts close to the wafer can easily reach the wafer surface. Examples of this sort are the dopant cross-contamination [2] and the iron contamination in implantations with heavy ions [3,4]. Implantations of wafers with exposed metal layers are suspected to be responsible for contamination of the implantation disk and as a consequence for contamination of wafers in subsequent implantations. In a recent paper [5] we showed that the implantation of wafers with an exposed tungsten layer is responsible for tungsten contamination of wafers implanted later. We set up a procedure to quantify tungsten contamination in ion implantation processes by DLTS (Deep Level Transient Spectroscopy), and used this procedure to evaluate the tungsten contamination and the efficiency of a decontamination process by implantation of dummy wafers. In the present paper we investigate more deeply this contamination, specifically the effect of the implantation energy, of the screen oxide and of the equipment setting. In a comparison among various techniques for contamination monitoring it was shown that DLTS is the best choice for slow diffusers [6], and for this reason we used DLTS in our study.

2. Experimental details

2.1. Sample preparation

P-type, (100), 200 mm diameter, 725 μm thick 10 Ω cm resistivity Magnetic Czochralski (MCZ) wafers were used in this study. Arsenic is known to be responsible for a relevant contamination by sputtering [3,4], and therefore arsenic implantations (10^{15} cm^{-2}, 60 keV) were used to monitor the contamination of the equipment after previous implantations of wafers with an exposed metal layer (tungsten). The implantations were performed in an Axcelis NV-GSD200EE/80 High Current ion implanter. The implanter is equipped with an Extended Life Source (ELS) source type, a 2D-SOLID silicon coated disk, and a Plasma Electron Flood (PEF) electron shower. PEF is used to avoid charging effects during ion implantation. This device is placed close to the process chamber and generates low energy electrons that are drawn into the beam. Low energy electrons are generated in a molybdenum arc chamber by ionization of a xenon gas by electrons coming from a tungsten filament. Electrons are extracted toward the beam (plasma bridge) with an energy $\leqslant$2.1 eV, depending on the implant application. The amount of emitted electrons depends on the beam potential (self-extraction) and assists in reducing the beam space-charge, the beam divergence and the beam potential before reaching the wafer.

The contamination induced by implantation was analyzed both under ordinary not-contaminated operation conditions and after contamination of the implanter by implantations of wafers with an exposed tungsten layer. The efficiency of a screen oxide layer (up to 150 Å thick) in reducing contamination was tested in two

* Corresponding author.
E-mail address: maria.polignano@st.com (M.L. Polignano).

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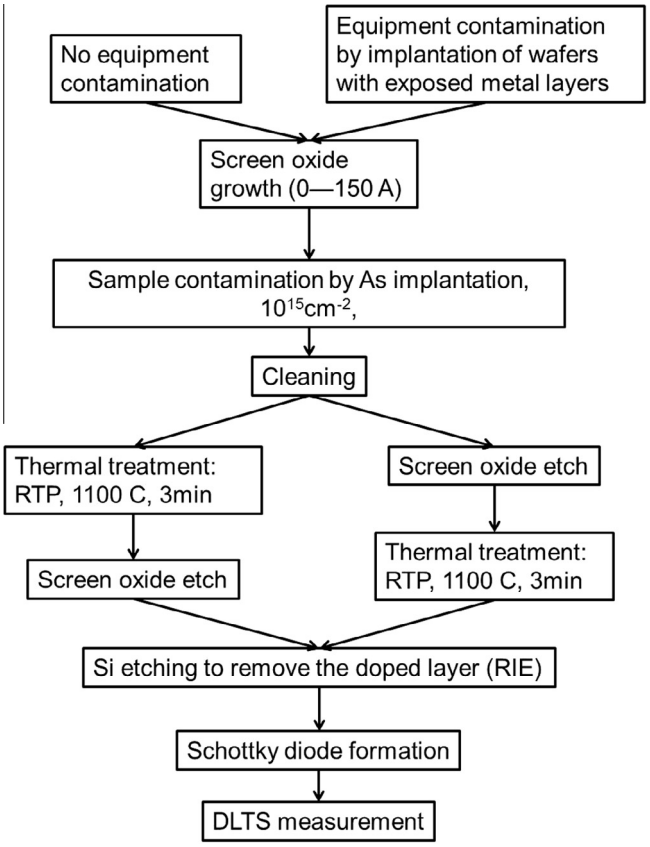
Table 1
Process flow used to prepare the samples for contamination monitoring experiments.



different process flows, i.e. by etching the oxide off before or after the thermal treatment. The ion energy is expected to be a relevant parameter in contamination by sputtering, and for this reason the impact of energy reduction (from 60 to 10 keV) was studied. The role of the PEF device was studied by varying the PEF arc voltage and the extraction voltage.

The flow used for the sample preparation is schematically reported in Table 1. After implantation, the metal surface concentration was measured by TXRF. Then, the wafers were cleaned by a conventional SC1–SC2 cleaning (Standard Cleaning 1 and Standard Cleaning2, [7]) and thermally treated by a Rapid Thermal Process (RTP) at 1100 °C for 3 min in an inert environment. This thermal treatment had the purpose to allow the contaminant diffusion in silicon. Then, the wafers received a Reactive Ion Etching (RIE) of 1.2–1.4 μm silicon with the aim to remove the doped layer. To obtain Schottky diodes for DLTS measurements, the native oxide was etched off and 1000 Å titanium layer was deposited on the silicon surface, masked and etched.

2.2. Experimental techniques

TXRF measurements were obtained by a RigakuTXRF300 instrument in direct mode, with the high energy beam at 0.05° angle and 500 s acquisition time for each point. The tool has a W filament working at 30 kV and 300 mA.

1 mm^2 area Schottky diodes were measured by DLTS. A Semilab DLS-83D instrument was used. In this instrument, lock-in integration is used for averaging capacitance transients, and temperature can be scanned in the range 30–300 K. Alternatively, constant temperature spectra can be obtained as a function of the frequency of excitation pulses in the range 0.5–2 kHz [8]. Both methods were used in this work.

The differential DLTS method was used. In this method, the Schottky diode (or the p–n junction) is reverse biased at a voltage V_r and two filling pulses are applied: the first pulse V_1 is applied at the beginning of the lock-in integration period, and a second pulse V_2 is applied a half period later. In the lock-in integration, the difference ΔC is obtained between the integrals of the capacitance transients caused by the first pulse and by the second pulse. The differential DLTS method can also be used to obtain the in-depth trap concentration profile. Indeed, this method yields the trap concentration in the interval $[x_d(V_1), x_d(V_2)]$, where x_d is the depletion region edge at a given reverse voltage. So by selecting appropriate values for V_1, V_2, and V_r, the trap concentration can be measured as a function of depth.

In our measurements, samples were reverse biased at −5 V, and filling pulses with amplitudes of −0.5 V and −4.5 V were applied with a pulse width of 20 μs during each integration period. Under these conditions, a region ranging from ~0.8 μm to 2 μm was analyzed. The spectra shown in this paper were obtained with a 23 Hz filling pulse frequency. When measuring the trap concentration profile, $V_1 - V_2$ was set at 0.5 V, with 6 V reverse bias. In any case, the region close to the surface cannot be analyzed by DLTS. In concentration profile measurements, V_1 can be positive to shrink the depletion region and acquire the trap concentration as close as possible to the surface; however, under our operating conditions reliable concentration data are obtained starting about 0.5 μm from the surface, down to 2.4 μm. Due to the sample preparation procedure, these depths correspond to 1.8–3.7 μm from the original wafer surface. The reverse voltage cannot be further increased because of Schottky diode leakage current issues, so the analysis cannot go deeper into silicon. The profile analysis is possible when the total trap concentration is high enough, and for this reason this analysis was carried out when the concentration estimated from the DLTS peak was larger than 10^{12} cm^{-3}.

3. Experimental results

3.1. Not contaminated equipment

Fig. 1(a) shows the DLTS spectra of a wafer implanted in a not contaminated implanter with 10^{15} cm^{-2} arsenic and 60 keV energy on the bare silicon surface. In these implantations the PEF arc voltage was 23 V and the extraction voltage was 2 kV. Two low concentration peaks are observed, and the corresponding Arrhenius plots of e_p/T^2 (where e_p is the hole emission rate and T is the absolute temperature measurement) are shown in Fig. 1(b). These peaks can be identified with molybdenum and tungsten by comparison with literature data [9,10], and are therefore labeled "H1–Mo" and "H1–W", respectively.

Fig. 2 reports the DLTS spectra of samples implanted with PEF arc voltage in the range 15–40 V and 2 kV PEF extraction voltage, and of samples implanted with PEF off. The samples implanted with arc voltage up to 23 V essentially have the same DLTS spectrum as the samples implanted with PEF off. Vice versa, an implantation with 40 V arc voltage results in a significant increase of the tungsten concentration, while the molybdenum concentration is unaffected. In addition, in the sample implanted with 40 V arc voltage one more peak is observed, located between H1, Mo and H1, W. This peak was previously observed [5] in tungsten-contaminated samples, and is here labeled H2, W. The peak H2, W will be better discussed in Section 3.2, where samples with a higher concentration of tungsten are analyzed, so that the tungsten peaks can be more reliably separated and identified. According to the data in [5], the concentration of H2, W is expected to be about 10–20%