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# Investigations on heavy ion induced Single-Event Transients (SETs) in highly-scaled FinFETs

M. Gaillardin [a,*], M. Raine [a], P. Paillet [a], P.C. Adell [b], S. Girard [c], O. Duhamel [a], F. Andrieu [d], S. Barraud [d], O. Faynot [d]

[a] CEA, DAM, DIF, F-91297 Arpajon, France
[b] Jet Propulsion Laboratory, Pasadena, CA 91101, USA
[c] Université de Saint-Etienne, Laboratoire H. Curien, UMR-5516, 42000 Saint-Etienne, France
[d] CEA, LETI-Minatec, 17 avenue des Martyrs, 38000 Grenoble, France

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ABSTRACT

We investigate Single-Event Transients (SET) in different designs of multiple-gate devices made of FinFETs with various geometries. Heavy ion experimental results are explained by using a thorough charge collection analysis of fast transients measured on dedicated test structures. Multi-level simulations are performed to get new insights into the charge collection mechanisms in multiple-gate devices. Implications for multiple-gate device design hardening are finally discussed.



## 1. Introduction

Multiple-gate transistors have been developed to push the limits of silicon-based devices towards the nanometer scale [1]. Several architectures such as FinFET [2], multiple-gate Field Effect Transistor (FET) [3], or planar double-gate transistors [4] have been proposed by several research teams to significantly reduce short channel effects and improve electrical performances compared to their single-gate counterparts. For a long time considered as academic devices, multiple-gate transistors and FinFETs are now included in mainstream applications. Indeed, Intel has recently introduced bulk Tri-Gate FETs to process Integrated Circuits (ICs) at the 22 nm node [5]. Radiation effects in those kind of devices have been studied since the early 90's [6–8]. Most studies based on experimental results were devoted to Total Ionizing Dose (TID) effects in multiple-gate transistors [9–14]. Others were dedicated to heavy ion induced micro-dose effects [15,16] but only few studies focused on Single-Event Effects (SEE) [17–19]. Experimental SEE studies on FinFET-based circuits are even more uncommon since only few publications have been published such as by Seifert et al. [20] on that topic. The objective of this paper is thus to get insights into the Single-Event Transient (SET) phenomena in FinFET devices as a function of the device design. Charge collection mechanisms are investigated using a statistical analysis of the charge collected on elementary devices irradiated with heavy ion broad beams. Then, the influence of the main geometrical device characteristics on the experimental data is presented. The impact of the amount of injected charge related to the incident particle Linear Energy Transfer (LET) and the effect of scaling are analyzed using both experimental and simulation results to separate all physical mechanisms which govern the SET response of multiple-gate transistors.

## 2. Experimental details

### 2.1. Test structures

Test structures are made of "Finger FET" named as FinFETs. In such devices, a silicon finger, named fin in the following, is wrapped into the gate stack leading to two or more conduction channels, as illustrated in Fig. 1. Table 1 summarizes main geometrical parameters: the physical gate length $L_G$, the fin width $W_{FIN}$, the fin thickness $T_{FIN}$ and the fin "length" $L_{FIN}$ which corresponds to the length between the gate-edge and the source-drain regions as described in Fig. 1.

* Corresponding author.
*E-mail address:* marc.gaillardin@cea.fr (M. Gaillardin).

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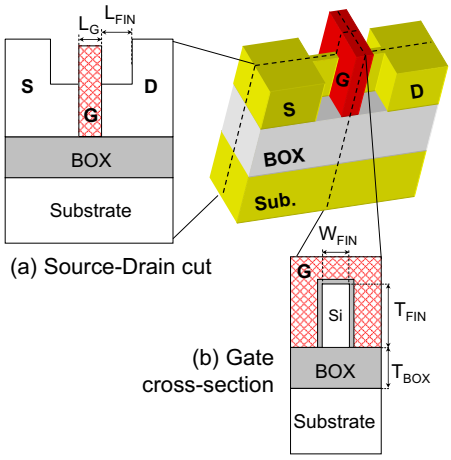


**Fig. 1.** Schematic description of SOI FinFETs and nanowires presented in (a) a cut along the channel direction named source-drain cut and in (b) a gate cross-section.

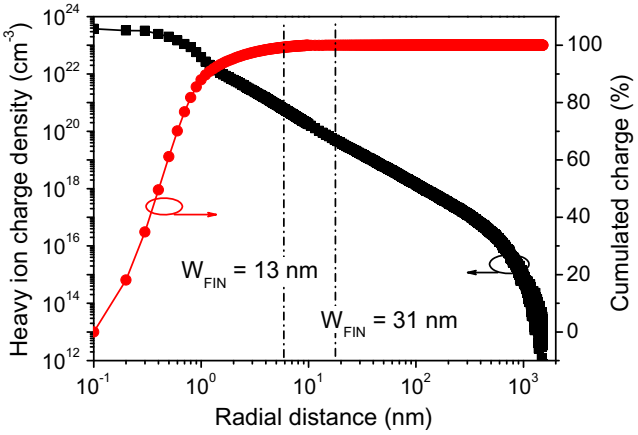


**Fig. 2.** Average charge density (black squares, left *y* axis) and the associated cumulated deposited energy (red circles, right *y* axis) generated by 5.5 MeV/amu $^{48}$Ca ions extracted from Geant4 simulations using MuElec extension. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

All tested devices are N-type transistors. FinFETs are processed with a lightly doped body ($\sim 10^{17}$ cm$^{-3}$) and a gate stack involving N+ polysilicon gates. These FinFETs are fabricated using a SOI substrate with a Buried OXide (BOX) thickness $T_{BOX}$ = 200 nm. The fin spacing ($\approx$250 nm), i.e. the distance between two neighboring fins, is sufficiently large to consider that the charge deposited by a heavy ion is significant only in the silicon fin directly struck by the heavy ion track core. This paper focuses on the influence of the main geometrical parameter ($W_{FIN}$, $L_G$) on the charge collection mechanisms. The impact of the heavy ion induced charge injection in devices' bodies is also analyzed using results gathered with various incident particle species.

### 2.2. Experiments

Devices are irradiated at the Grand Accelerateur National d'Ions Lourds (GANIL), Caen, France, with heavy ion broad beams using either $^{48}$Ca ions with 5.5 MeV/amu incident energy or $^{86}$Kr ions with 9 MeV/amu incident energy. These two beams correspond to a Linear Energy Transfer (LET) of 15.9 and 32.7 MeV cm$^2$/mg respectively at their entrance in the device under test. Irradiations are performed either in vacuum or in air, always at normal incidence. These heavy ions are specifically chosen since most of their energy is deposited in the first nanometer around the ion path as shown in Fig. 2 where the generated average charge density is plotted for a 5.5 MeV/amu $^{48}$Ca ion, as a function of the radial distance to the ion path (black squares, left *y* axis). Such a "heavy ion track" which exhibits a huge electron/hole pair density close to the heavy ion track core, but it dramatically decreases after only few nanometers. This figure is the result from Monte Carlo simulations performed with Geant4 [21,22], using the MuElec extension [23,24] (see [25] for more details on the simulation procedure). Fig. 2 shows that the total energy deposited in the narrow ($W_{FIN}$ = 13 nm) and the ($W_{FIN}$ = 31 nm) wide FinFET are then close to each other as highlighted by the cumulated energy deposition curve (Fig. 2, red circles, right *y* axis). According to this figure, the difference between the total deposited energy deposited in a narrow and a "wide" FinFET is limited to only few percent. If any discrepancy were observed between the collected charges of various FinFET geometries, it could not be attributed to the amount of generated charge in the active silicon finger.

The experiments are performed using a setup dedicated to direct measurement of current transients, close to the one described in [26]. FinFETs are mounted on High Frequency (HF) packages which are welded on HF cards. Devices are OFF-biased through a bias-T during experiments, meaning that only the drain electrode is biased to the nominal voltage $V_{DD}$ = 0.9 V and all other terminals are grounded. For each irradiation run, more than 200 current transient waveforms are recorded on a high performance single-shot oscilloscope. Collected charges are then calculated by integrating the current transient over time, taking a great care to avoid integration errors due to both high and low frequency noises. High fluxes (several $10^7$ ions cm$^{-2}$/s), such as those accessible at GANIL, are mandatory to get sufficient statistics in a reasonable time since the sensitive area of FinFET devices is extremely reduced.

Results from these experiments are presented in the following sections, each section being dedicated to the impact of one particular geometrical characteristic of the fin on charge collection mechanisms.

**Table 1**
Main geometrical parameters of FinFETs tested for this study.

| Type | $W_{FIN}$ | $L_G$ | $L_{FIN}$ | $T_{FIN}$ |
|---|---|---|---|---|
| FinFET | 13 nm (±2 nm) | 55 nm | 150 nm | 80 nm |
| FinFET | 20 nm (±3 nm) | 55 nm 1 μm | 150 nm | 80 nm |
| FinFET | 31 nm (±3 nm) | 55 nm | 150 nm | 80 nm |

### 2.3. Impact of fin width on charge collection mechanisms

Effects of the FinFET design on the SET response have been recently investigated in [19]. In this reference, the results showed that the heavy-ion induced current transient could be significantly mitigated when FinFETs are designed using saddle contacts instead of dumbbell contacts. In this paper, we focus on the design and the geometry of the silicon fin itself to get insights into potential specific charge collection mechanisms and to improve SETs mitigation in FinFET devices and ICs.

### 2.4. Experimental charge collection distributions depending on the fin width

The main feature of multiple-gate devices based on the FinFET architecture is the presence of lateral gates allowing a better control of the electrostatic potential in the silicon finger than in classical single-gate transistors. Reducing the distance between the