Nuclear Instruments and Methods in Physics Research B 365 (2015) 636–640

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research B

journal homepage: www.elsevier.com/locate/nimb

Dispersion of heavy ion deposited energy in nanometric electronic devices: Experimental measurements and simulation possibilities

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ARTICLE INFO

Article history:
Received 27 May 2015
Received in revised form 1 September 2015
Accepted 29 September 2015
Available online 22 October 2015

Keywords:
Monte Carlo simulation
Deposited energy
Nanometric volumes
Geant4
Microelectronics

ABSTRACT

The dispersion of heavy ion deposited energy is explored in nanometric electronic devices. Experimental data are reported, in a large thin SOI diode and in a SOI FinFET device, showing larger distributions of collected charge in the nanometric volume device. Geant4 simulations are then presented, using two different modeling approaches. Both of them seem suitable to evaluate the dispersion of deposited energy induced by heavy ion beams in advanced electronic devices with nanometric dimensions.

1. Introduction

When studying heavy ion induced Single-Event Effects (SEE) in electronic devices, the Linear Energy Transfer (LET) is generally used as the main parameter to characterize the incident beam. This LET metric is assumed to reflect the energy deposited by each incident ion in the sensitive volume of the studied device. The sensitivity of a particular device is then determined using a LET threshold criterion for the triggering of a given type of effect. Yet, this average metric does not reflect the stochastic nature of particle-matter interaction, and the resulting intrinsic dispersion of energy deposited by direct ionization events [1,2]. Indeed, two ions of a given beam, with same species and same energy, will have two different paths in matter and will thus deposit two different values of energy. Electronic technology scaling comes with thinning active silicon layers, resulting in devices getting more and more sensitive to the scattering mechanisms of ion-matter interactions. This sensitivity should be particularly pronounced in Silicon On Insulator (SOI) technologies, in which the active silicon film collecting the deposited energy is electrically isolated from the substrate by an insulating layer of buried oxide. Previous work actually showed large experimentally measured deposited energy dispersion, increasing with silicon film thickness decrease [3]. In this previous work, devices were chosen with thin active layers but large lateral dimensions, to capture the entire radial dimension of the ion track. There is now a need to quantify this deposited energy dispersion for advanced devices with nanometric sensitive volumes, i.e. thin layers and limited lateral dimensions, such as SOI FinFETs.

Another issue lies in the possibility to take into account this deposited energy dispersion in simulation studies. While Monte Carlo codes are by definition well suited to address the statistical nature of interaction mechanisms of ions in matter, most of them actually present some limitations when dealing with thin layers of material. They indeed often use simplifications or condensed history approaches to optimize the calculations, thus limiting the simulation accuracy for small dimension geometries, and averaging in particular the energy loss dispersions. Fluctuations models are then used to compensate for this limitation, but it is not clear how well these models succeed for capturing energy loss phenomenon in thin layers. This could become a crucial issue at the nanometer scale involved in modern devices.

This work first proposes to experimentally quantify the amount of deposited energy dispersions for advanced SOI FinFET devices, with nanometric dimensions. Geant4 Monte Carlo simulation of deposited energy dispersion is then presented, exploring the possibilities of different simulations approaches, using either traditional condensed history approximations, or recently implemented discrete energy loss models, called MicroElec.

2. Devices under test

Both SOI FinFET transistors and SOI diodes are used to investigate the dispersion in the heavy ion energy deposition during radiation tests.

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http://dx.doi.org/10.1016/j.nimb.2015.09.087
0168-583X/

A FinFET device processed by CEA-LETI is used to study the heavy ion energy deposition in a nanometric sensitive volume. Fig. 1 illustrates the geometry of this kind of device, in which a silicon finger is wrapped into the gate stack, thus limiting the collection volume to nanometric dimensions. The main geometrical parameters delimiting this volume are summarized in Table 1: the gate length L_{Si}, the fin width W_{Si} and the fin thickness T_{Si}. According to previous experimental results [4], this device seems to present almost no bipolar amplification; the collected charge value can thus be considered very close to the generated charge value, directly related to the deposited energy.

In addition, a large diode is also used, with a same order of magnitude active silicon film thickness as the FinFET device. It will serve as a reference to calibrate the Monte Carlo simulation on thin layers but infinite lateral dimensions, before simulating nanometric volumes. This diode is fabricated in a 70 nm partially depleted (PD) CMOS/SOI technology processed by CEA-LETI. The size corresponds to the nominal gate length of the transistors fabricated with the same process [5,6]. For SOI devices, the sensitive volume is electrically isolated from the substrate by the buried oxide, thus limiting the collecting film thickness. The Unibond fabrication process of this diode also ensures a good control over the uniformity of the silicon film. The thickness variation is indeed estimated to be ±5% [7] across a whole wafer, and will be even smaller across a single device. This device is chosen with large sensitive area, that can be considered infinite compared to the heavy ion track, i.e. all energy is deposited in the device and collected. The main technological characteristics and dimensions are reported in Table 1. During irradiation, the SOI diode is reverse-biased; in this configuration, the entire energy deposited in the sensitive volume is collected. Moreover, the diode structure ensures the absence of charge amplification.

3. Experimental setup

Heavy ion irradiations are performed at the Grand Accelerateur National d'Ions Lourds (GANIL), Caen, France. Different monoenergetic broad beams of different ion species are used. The main beam characteristics are reported in Table 2. Irradiations are performed in a vacuum chamber or in air, at normal incidence. A direct measurement technique (Fig. 2) similar to the one described in [9] and optimized for high bandwidth measurements is used to record the current transient pulses triggered by the heavy ions in irradiated transistors and diodes. The drain of devices is biased through a bias-T; all other terminals are grounded. For each irradiation run, more than 200 current transients are recorded on a single-shot high bandwidth oscilloscope. Collected charges are then calculated through integration of the current transients over time. Only one device is used for each type of tested component, to avoid the additional effect of device-to-device variations that might increase the measured dispersions.

Table 1
Main technological characteristics of the tested devices.

Technology	Device	Supply voltage (V)	Sensitive area	T_{Si} (nm)
PD SOI – 70 nm	Diode	0.7	$5 \times 200\ \mu m^2$	150
FinFET	Transistor	0.9	$20 \times 90\ nm^2$	80

Table 2
Main characteristics of the GANIL incident ion beams used in this study, at the entrance of the studied devices. The LET is calculated in silicon with SRIM [8].

Ion	Energy (MeV/amu)	LET (MeV cm^2/mg)
^{86}Kr	50	12.0
^{48}Ca	5.5	15.9
^{86}Kr	9	32.7

4. Experimental results

The metric measured during these experiments is a dispersion of collected charge in the different tested devices, for different ion species and energies, corresponding to different values of theoretical LETs. Because of the devices chosen for this study, these measured collected charge values can be directly related to the values of deposited energy. The results are reported in Figs. 3 and 4 for the diode and FinFET respectively, as a number of ion-induced transients as a function of measured collected charge. These last values have been normalized to the respective silicon film thickness of the two devices and expressed in units of fC/nm, to allow more direct comparison between different thicknesses and with the theoretical LET value. The percentage of transients itself is only indicative; it depends on the chosen histogram binning and oscilloscope settings such as the trigger level. The main characteristics of the measured distributions are reported in Table 3. The theoretical LET values, expressed in fC/nm, are also reported, for comparison with the average of the measured distributions.

The measured collected charge average values, normalized to the silicon film thicknesses, are consistent with the theoretical LET values, only slightly lower. Similar values are also measured for both kinds of devices, with slightly lower values in the FinFET

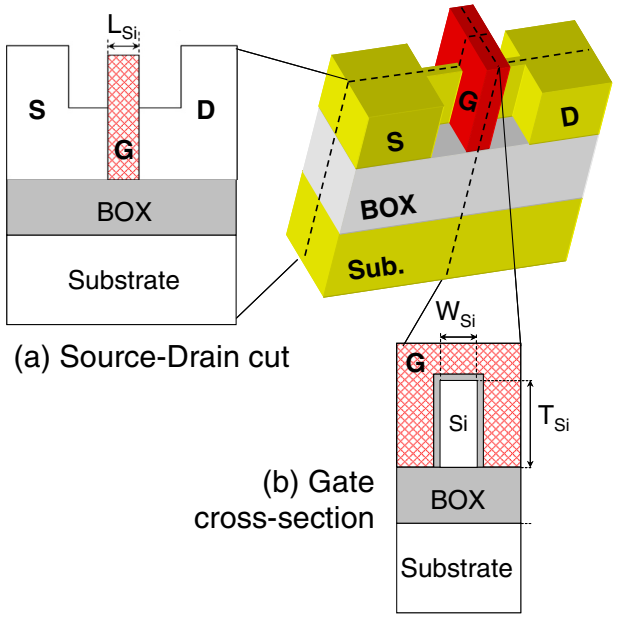

Fig. 1. FinFET schematic with (a) source–drain cut and (b) gate cross section.

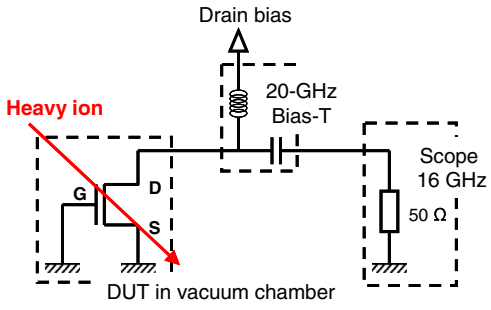

Fig. 2. Experimental setup.