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# *C–V* and DLTS studies of radiation induced Si–$SiO_2$ interface defects

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ABSTRACT

Interface traps at the Si–$SiO_2$ interface have been and will be an important performance limit in many (future) semiconductor devices. In this paper, we present a study of fast neutron radiation induced changes in the density of Si–$SiO_2$ interface-related defects. Interface related defects ($P_b$ centers) are detected before and upon the irradiation. The density of interface-related defects is increasing with the fast neutron fluence.



## 1. Introduction

Over the past several years one of the most expanding research field in the area of nanoelectronics are three-dimensionally confined semiconductor nanocrystals in the oxide matrix. The reason is their promising application in nonvolatile memories [1] and third generation solar cells [2]. The number of studies dealing with electrical properties is increasing, and among them the capacitance–voltage measurements (*C–V*) of metal-oxide-semiconductor (MOS) structures containing Si or Ge nanocrystals have attracted a considerable attention. Recently, it has been shown, that semiconductor–oxide interface has a strong influence on charge trapping properties of Ge nanocrystals in $SiO_2$ matrix [3]. Moreover, it has been proposed to use reactor neutron flux for doping Ge nanocrystals in $SiO_2$ matrix [4]. While irradiation with thermal neutrons leads to doping of nanocrystals, irradiation with fast neutrons leads to appearance of radiation-induced damage. The interest in neutron transmutation doping (NTD) comes from one of its main advantages over the other methods for doping. It is high-precision doping, because the concentration of impurities introduced at a constant neutron flux is proportional to irradiation time [5]. The question that arises is what is the influence of radiation-induced defects on "as-grown" interface-related defects in such systems? In particular, defects introduced with fast neutrons irradiation. It has been known for many years that MOS structures are extremely sensitive to radiation because electrically charged defects build up in the oxide layer. However, an overview of the literature data showed that most of studies were dealing with X and $^{60}Co$ gamma rays [6]. The influence of reactor neutrons is still unclear.

In this work, we present a preliminary study of reactor neutrons irradiation induced interface-related defects in Si–$SiO_2$ structures. We have taken the Si–$SiO_2$ structures without semiconductor nanocrystals in the oxide. Furthermore, we have eliminated thermal neutrons (as much as possible) with cadmium shields in the reactor, as they will be used only for doping of nanocrystals. This paper addresses two issues: (1) what is the influence of fast neutron irradiation on Si–$SiO_2$ interface related states, and (2) how can we study those states by the means of DLTS.

## 2. Experimental details

The single crystal Si(100) substrate used in this study was prepared by Cemat Silicon S.A. (Warsaw, Poland). The substrate was phosphorous-doped with initial resistivity in the range 10–20 Ω cm. $SiO_2$ film was thermally grown at an oxidation temperature of 1000 °C in a [$H_2 + O_2$] atmosphere (wet oxide). The obtained oxide thickness was 50 nm.

The samples were irradiated with 0.7 MeV neutrons in the carousel facility (CF) of the TRIGA Mark II reactor of the Jozef Stefan Institute in Ljubljana, Slovenia. Neutron irradiations were done inside a cadmium box with thickness of 1 mm to filter out the thermal neutrons. The effective cut-off energy of Cd is 0.55 eV, with distribution maximum for fast neutrons at 0.7 MeV [7]. The flux of fast neutrons was constant at $2.6 \times 10^{10}$ $cm^{-2}$ $s^{-1}$, and the accumulated fluences were $1.6 \times 10^{12}$, $7.8 \times 10^{12}$ and $1.6 \times 10^{13}$ $cm^{-2}$. The temperature of the samples during irradiation did not exceed 30 °C.

For the gate metallization Au was used. The MOS capacitor area was 0.8 $mm^2$. High-frequency *C–V* characterization was performed at different temperatures. All DLTS spectra were taken with a SULA Technologies spectrometer.

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## 3. Results and discussion

Fig. 1 shows high-frequency (1 MHz) *C–V* measurements at room temperature for all samples. The samples are referred to as $S_{asprep}$ (as prepared), S-IR-1 (irradiated with the fluence of $1.6 \times 10^{12}$ cm$^{-2}$), S-IR-2 (irradiated with the fluence of $7.8 \times 10^{12}$ cm$^{-2}$) and S-IR-3 (irradiated with the fluence of $1.6 \times 10^{13}$ cm$^{-2}$) in the following text (Table 1). This steplike form or "S-shape", observed for all samples, is typical for the MOS structures on n-type Si substrate in the case of high frequency measurements [8]. For the positive voltage the capacitance reaches its maximum value (accumulation region), while for the negative voltage the capacitance is reducing to the minimal value (inversion region). No significant changes have been detected upon irradiation in samples S-IR-1 (Fig. 1b) and S-IR-2 (Fig. 1c), while the most considerable changes (in depletion region) have been observed in the S-IR-3 sample (Fig. 1d), i.e. upon irradiation with the highest fluence. It is known that, for small positive gate voltages, the surface is depleted and the space-charge region charge density dominates. Trapped interface charge capacitance also contributes. The total capacitance in depletion region is the combination of $C_{ox}$, $C_b$ and $C_{it}$ [9], where $C_{ox}$, $C_b$ and $C_{it}$ are oxide, substrate and interface capacitances, respectively. The changes in $C_b$ are expected to be minimal, as explained later, so we strongly believe that changes observed in the S-IR-3 sample (Fig. 1d) are mostly interface and/or oxide related. The more detailed separation of those contributions is not possible.

Information regarding the energy distribution and the density of traps are crucial for the future device applications. To obtain those information deep level transient spectroscopy (DLTS) could be used. The DLTS is a well established technique which is commonly used in studying the trap states in the semiconductors [10], and recently it has been applied in studying the semiconductor nanocrystals [11]. However, it is well known that application of DLTS to study interface-related defects is extremely difficult due to the several reasons. The most important are:

(i) The capacitance base line shift; DLTS signal is measured as a function of temperature (usually in a range from liquid nitrogen temperature to room temperature). The scanning of the temperature causes a change in the capacitance signal due to the thermal dependence of the electron emission rate. The important assumption is $\Delta C \ll C$ i.e. the measured traps make only a small contribution to the sample total capacitance. This is not the case for the interface traps.

(ii) Fermi level pinning effect; the shift of the accumulation region to higher voltages (observed for MOS structures) has been explained by the Fermi level pinning effect. The magnitude of the Fermi level pinning depends on temperature. More details regarding those issues are given elsewhere [12,13].

**Table 1**
The Si–$SiO_2$ samples description with associated fast neutron fluence. Activation energies ($\Delta E_a$) and densities ($D_{it}$) of interface-related defects estimated from the DLTS.

| Sample | Neutron fluence (cm$^{-2}$) | $\Delta E_a$ (eV) | $D_{it}$ (eV$^{-1}$ cm$^{-2}$) |
|---|---|---|---|
| $S_{asprep}$ | – | 0.27 ± 0.01 | $1.9 \times 10^{11}$ |
| S-IR-1 | $1.6 \times 10^{12}$ | 0.27 ± 0.02 | $7.7 \times 10^{10}$ |
| S-IR-2 | $7.8 \times 10^{12}$ | 0.27 ± 0.01 | $1.3 \times 10^{11}$ |
| S-IR-3 | $1.6 \times 10^{13}$ | 0.23 ± 0.01 | $1.4 \times 10^{11}$ |

We have performed *C–V* measurements at low temperatures (250, 200 and 150 K) in order to check the Fermi level pinning effect, but significant shift of the accumulation region to higher voltages has not been observed. It implies that the density of interface related traps is not too high, as the shift of the accumulation region is directly connected to the density of interface traps.

Taking into account all the facts, we have selected temperature interval (100–180 K) and the optimal voltage settings (bias at 0 or −1 V) for DLTS measurements. The voltage settings have been chosen in order to make the capacitance signal coming from the interface to be the most important [9].

Fig. 2 shows DLTS spectra for all samples at the same rate window, $\tau = 5$ ms. Only one trap with temperature maxima at 123, 142, 152 and 145 K for the $S_{asprep}$, S-IR-1, S-IR-2 and S-IR-3 sample, respectively, has been detected. Irradiation did not introduce new traps in DLTS spectra. Activation energies of electron emission have been determined from Arrhenius plot of $\ln(e_n/T^2)$ versus $1/kT$ as 0.27, 0.27, 0.27 and 0.23 eV for the $S_{asprep}$, S-IR-1, S-IR-2 and S-

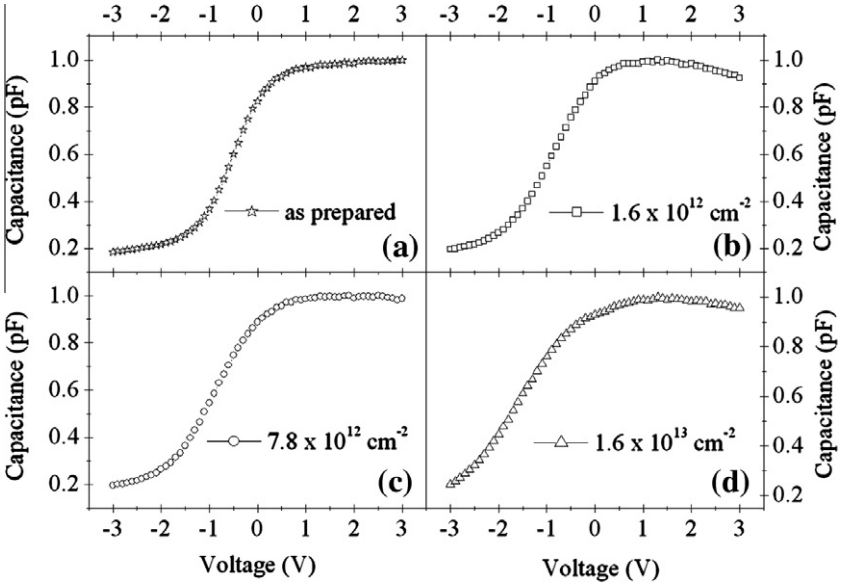


**Fig. 1.** The normalized (1 MHz) *C–V* measurements at room temperature for all samples: (a) as prepared MOS structure, (b) irradiated with neutron fluence of $1.6 \times 10^{12}$, (c) irradiated with neutron fluence of $7.8 \times 10^{12}$ and (d) irradiated with neutron fluence of $1.6 \times 10^{13}$ cm$^{-2}$.