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Data acquisition for the Combined Ion and Neutron Spectrometer (CINS)

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ABSTRACT

The CINS (Combined Ion and Neutron Spectrometer) consists of three detector systems: a boron-loaded plastic scintillator for medium energy neutrons, a silicon detector system for high-energy neutrons, and a charged particle stack containing both silicon detectors and scintillators. A readout system built for the charged particle stack is described here. The stack must be able to detect particles over a wide range of charge and energy. It contains 7 detectors, including 4 silicon detectors that each have two output paths. The readout must have a large usable dynamic range and must be able to handle the relatively high event rates that occur when the stack is placed in an accelerator beam. The data acquisition system detects events (that is, compares incoming signals to user-supplied trigger definitions), proceeds to capture waveform data from the preamplifiers, and saves the data to a hard drive. Although only used with the charged particle stack to date, the system can also be used with the other elements of CINS.

1. Introduction and requirements

The charged particle stack in CINS (the Combined Ion and Neutron Spectrometer) is described in detail in the accompanying article [1]. CINS consists of a silicon telescope to measure charged particles, additional silicon detectors with anti-coincidence detectors to measure high-energy neutrons, and a large scintillator made of borated plastic. CINS is intended for use at accelerator facilities to make measurements of interest to the space radiation community, including shielding studies and measurements of fragmentation cross sections. With some re-packaging, as proposed in [1], the mass, volume, and power consumption could be reduced to make CINS a viable instrument package for human flight. Here we describe a custom, flexible readout system built to accommodate all the CINS electronics channels. It can also be used with other signal sources if desired. The custom system largely eliminates the need for older, bulkier readout hardware (NIM, CAMAC, VME). Although it has not been optimized for spaceflight, it can be considered a mid-point between traditional nuclear electronics and the electronics that would be used in a flight instrument.

The four silicon detectors that comprise the bulk of the charged particle stack each have a high-gain and low-gain output, requiring 8 readout channels. The other components of the stack are two plastic scintillators and a fairly thick BGO crystal intended primarily to stop protons with energies below about 150 MeV. The three scintillators bring the channel count to 11. To accommodate these channels and allow room for expansion (which would mean incorporation of four or five neutron detector signals), a 16-channel system was designed and built.

The wide dynamic range of the signals coming from the detector electronics require ADC resolution of 14 bits or more, sampled at 10 MHz or higher. The dynamic range requirement flows from the wide range of particle types and energies encountered in space, and also at accelerators where high-energy heavy ion beams are produced. The data acquisition electronics must detect valid trigger conditions from the incoming signals and save event data to disk. An event is triggered when the signal level on a given channel increases by a user-specified value within eight 10 MHz samples or less. When an event is detected, the system saves the previous 64 ADC (Analog to Digital Converter) samples and the next 64 ADC samples on all channels, as described in more detail below. The samples prior to the trigger are used to determine the baseline, or pedestal, in the time just prior to the particle hit. In low-rate conditions, the baseline should be stable, but when the rate is such that pulses from consecutive events can overlap, the baseline may not always be at its nominal level, and hence it is useful to retain the pre-trigger samples.

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The maximum trigger rate is assumed to be 1 kHz, making the maximum data rate 4 MB/sec. There are two optional additional constraints to declare a valid event, referred to as coincident and anti-coincident. Data collection only occurs if all user-specified coincident channels trigger within eight 10 MHz clock cycles. Requiring an event to occur on multiple channels simultaneously eliminates noisy or otherwise invalid data. Each channel specified by the user to be anti-coincident prevents data from being collected for the next eight 10 MHz samples.

2. Implementation

The Analog Devices AD9259 ADC was chosen because it provides 14 bits and will run at speeds in excess of 10 MHz. The AD9259 also contains 4 channels per chip with serial data to reduce the pin count required for the FPGA. The AD9259 requires a clock at the sampling rate. The clock is internally multiplied by seven with dual-edge clocking to provide serial data output at the sample rate. The signals are transmitted using LVDS (Low Voltage Differential Signaling). To reduce the design effort required, the AD9259-EZB evaluation board was used. This board contains an ideal layout for the ADC along with power supply noise rejection, input analog electronics, and single ended to differential clock conversion. The board also allows for some limited mode configuration for on-chip test pattern generation for debugging purposes. Four AD9259-EZB boards were used for this program to provide 16 channels of data. Because waveforms are recorded for later analysis, no peak detect-and-hold circuitry is needed.

To achieve the required data rate, the Opal Kelly XEM3001 board was chosen to interface between the ADCs and the GSE (Ground Support Equipment) computer. The XEM3001 consists of a USB controller chip, a PLL clock source and a Xilinx Spartan 3 FPGA. USB is capable of up to 40 MB/s, easily satisfying the data rate requirement. The clock source can generate the required 10 MHz. The Xilinx Spartan 3 FPGA is large enough to perform the data buffering and trigger logic required. Finally, a custom board was designed to integrate the XEM3001 with the four AD9259 evaluation boards. This board routes the LVDS signals to IO pins on the FPGA, terminates the LVDS and distributes the 10 MHz clock. A picture of the evaluation boards, the Opal Kelly board, and connection board is shown in Fig. 1. The front panel has 16 feed-through BNC connectors for the analog signals, along with a USB connector, a manual reset switch, and power supply terminals for connection to the DC power supply. The present size of the box is large but it could easily be greatly reduced.

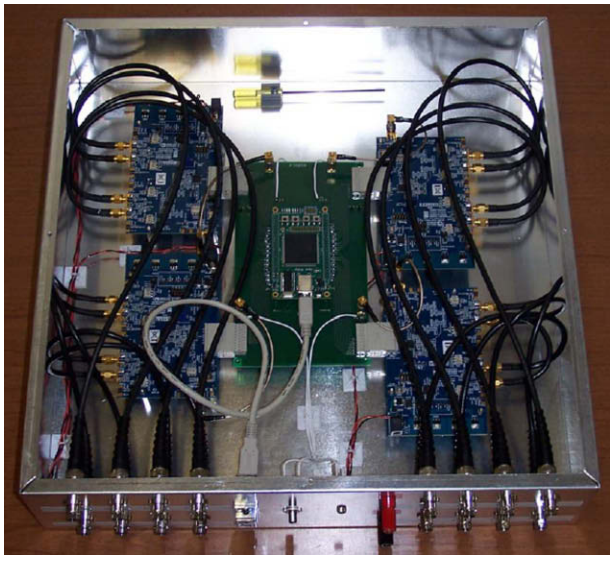

Fig. 1. The ADC evaluation boards, Opal Kelly board, and connection board in their housing.

3. FPGA design

Opal Kelly provides VHDL hardware modules that can be implemented in the FPGA design. These modules facilitate the transfer of data from the GSE computer to the FPGA through their software driver that contains C++ functions. The combination of the VHDL modules and C++ function calls trivializes the USB interface, simplifying it to a series of registers and FIFO buffers. The registers are used for transferring small data words when prompted by the GSE user through what Opal Kelly calls "wires". Some FPGA register controls include: hardware reset; front panel LED, and start data acquisition. Other wires implemented will be explained below. The FIFO buffers are used for transferring data at high rates through what Opal Kelly calls "pipes." Specifically this design uses "block throttle pipes" for the fastest possible data transfer rate.

Each of the data lines from the 16 ADC channels is sampled by the FPGA with the 70 MHz clock provided by the AD9259. There are two shift registers for each channel, one sampling on the rising edge of the clock and one sampling on the falling edge. Once seven bits are sampled from each channel within a single valid frame signal, the complete 14 bit word is placed in a buffer. This 128 word deep buffer is written continuously and stores a complete event for all channels.

In the case of a simple single-channel trigger, the event processing is as follows. The trigger value, entered by the GSE user at the start of a run, is loaded into a register in the FPGA using the Opal Kelly wires interface. After the present sample is written to the buffer, it is compared to the sample written to the buffer 8 clocks earlier. If the current sample is larger than the earlier sample by more than the value specified by the trigger value, an event is considered to have occurred, and the previous 64 samples and the next 64 samples taken are defined to be an event on this channel. All 16 buffers (one per readout channel) of 128 samples are written to a larger USB buffer, which is downlinked to the computer through the Opal Kelly pipe interface. This FIFO buffer is 255 bits wide and 512 words deep, making room for 4 event buffers. If there is not enough room in the USB FIFO for a complete event, the event is discarded. Registers accessible by software indicate how many triggered events were taken and how many were discarded per run. This provides a direct measurement of the livetime. A block diagram of the register and FIFO structure in the FPGA is shown in Fig. 2.

There is additional trigger logic for configurations where the coincident and anti-coincident constraints must be met. When any given channel that is defined to be part of the coincidence triggers an event, the least significant bit of an 8 bit shift register for that channel is set. This defines the beginning of an eight sample trigger window. The other channels defined by the GSE user as coincident must trigger within the trigger window for the single channel event to cause a system event and cause the data to be saved. A similar set of registers exists for anti-coincident channels. When an event occurs on an anti-coincident channel, the least significant bit of an eight bit shift register is set. Any triggers present on any other channels are ignored until this event clears through the shift register. A block diagram of this logic is shown in Fig. 3.

The FPGA design also contains a test pattern generator, enabled by the GSE user, for debug and testing when no input waveform is available. The test pattern fills the 128 sample buffer with an incrementing count pattern at 10 MHz. This would be too fast for the USB link to download, so an artificial trigger rate is also generated