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ScienceDirect

Nuclear Instruments and Methods in Physics Research B 260 (2007) 264–269

NIM B
Beam Interactions
with Materials & Atoms

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Ion beam induced charge (IBIC) studies of silicon germanium heterojunction bipolar transistors (HBTs)

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Abstract

SiGe HBTs are strong candidates for space communication applications because of their resistance to total dose effects and their overall high performance. However, they seem to be sensitive to single event upsets (SEUs). These devices were designed using deep trench isolation geometry to reduce charge collection due to ion hits outside the active area. Using four electrode (base, emitter, collector, and substrate) IBIC measurements at the Sandia Nuclear Microprobe Facility, we found that the largest fraction of the induced charge occurred on the collector and on the substrate; significantly less induced charge was found on the base electrode, and practically no induced charge was detected on the emitter. These devices showed a very well defined, high charge collection area enclosed by the deep trench. There was a sudden drop of induced charge at the trench but a long tail was present outside of the active area extending several tens of microns. The charge collection mechanisms inside and outside of the deep trench will be discussed and first results of Time Resolved IBIC in SiGe HBTs will be presented.

PACS: 81.05.Hd; 61.80.−x; 81.40.Wx

Keywords: IBIC; TRIBIC; SiGe; Radiation effects; Single event upset

1. Introduction

Most of today's electronics is based on silicon. Silicon has many advantages over other semiconductors. It is available in large amounts and can be purified to very high grade ($<10^{10}$ impurities/cm^3). It can be grown into large, defect-free single crystals and can be easily doped with either n-type or p-type impurities in a high dynamic range. One of the most important properties of silicon is that an extremely high quality dielectric (SiO_2) can be grown on it using simple methods. Silicon is a perfect material for system-on-chip (SOC) technology since several different kinds of devices can be built on the same chip. Analog (bipolar junction transistors (BJTs)) and digital (metal-oxide-semiconductor field emission transistors (MOS FETs)) devices can be manufactured and connected on the same wafer. Unfortunately, silicon has its limitations. The carrier mobility in silicon is relatively small; it saturates around 10^7 cm/s at high electric fields. Also, since silicon is an indirect bandgap semiconductor, it has very low light emission efficiency. The communication industry today requires higher speeds and high levels of integration for its integrated circuits (ICs) at low cost. In addition, the space industry wants to find an IC technology that is radiation hard for space application without additional radiation hardening which usually leads to increased cost, speed degradation, and area penalty. An alternative to

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[1] Sandia is a multi-program laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under Contract DE-AC04-94AL85000.

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0168-583X/$ - see front matter © 2007 Published by Elsevier B.V.
doi:10.1016/j.nimb.2007.02.032

the silicon technology are devices based on the III–V semiconductors, such as GaAs. These devices have the carrier mobility required for high speed ICs, and due to the way they are fabricated, they allow bandwidth engineering which is beneficial for optical devices. But there are practical disadvantages as well of these materials. First of all there is no robust thermally grown oxide for these materials. The single crystal wafers are also generally smaller compared to the silicon ones, and they have much higher defect density and poorer thermal and mechanical properties. All these lead to lower yields and consequently to higher cost. The III–V semiconductor technology has its place in the world of electronics, but it will never become a mass production technology if silicon based technologies can achieve or even approach the performance levels that these other technologies offer.

A promising new technology that combines the high speed of the III–V semiconductors with the well established and easy manufacturing processes of silicon is based on SiGe. The SiGe alloy allows the bandgap engineering of silicon devices while keeping the same fabrication technology developed for silicon devices; therefore, the analog BJTs can be easily combined with digital CMOS devices on the same wafer. These new devices are very promising; a current, very detailed review of the technology and the characteristics can be found in [1]. The SiGe HBTs can perform comparably to the III–V devices, and an additional bonus is that they were shown to be extremely radiation hard considering total dose and displacement damage [1]. However, it was shown through experiments [2,3] and simulations [4] that these devices can be vulnerable to single event upsets (SEUs). SEUs are changes in the logical state of a circuit due to the current induced in the device by the movement of the carriers created by an incident heavy ion. In order to understand the mechanism of SEUs it is necessary to study and understand the ion beam induced charge induction in the device. This study can be done through simulation using various device codes or experimentally using the ion beam induced charge/current (IBIC) technique. The simulations are usually compared to the experiments to calibrate/validate the calculations. We used the Sandia National Laboratories (SNL) nuclear microprobe facility to perform IBIC experiments on various SiGe HBT structures. Simulations were carried out to model the spatial distribution of the IBIC signal (induced charge). Finally, we performed the first Time Resolved IBIC (TRIBIC) experiments on these structures. The TRIBIC results provide more information for the simulation validation/calibration since they measure the induced current/charge as a function of time instead of only the total induced charge as the IBIC experiments do.

2. Experimental

In these experiments we used SiGe HBTs from various vendors, but they basically had the same structure as shown in Fig. 1. All the devices underwent chemical vapor etching to remove all but about 7 μm of the dielectric and metallization stack. This process allowed the ions to penetrate deeper into the device. For these experiments a beam of 36 MeV oxygen ions was focused into a 1 μm^2 spot and scanned over generally a $50 \times 50\ \mu m^2$ area. These oxygen ions have a range of 25.5 μm and deposit a total of ∼1.7 pC of charge in silicon. All four electrodes (collector, base, emitter, and substrate) were connected to amplifier chains consisting of Ortec 142A charge sensitive preamplifiers and Ortec 671 spectroscopy amplifiers. In addition, the signals were fed into individual SCAs which were then connected to a four input OR logical unit. The output of the logical OR unit was connected to the gates of the ADCs for the *X*–*Y* scan generator's output that were operated in SVA mode. All the ADCs were connected to a FastCom MPAWIN multi-parameter system. This way a signal on any of the four channels triggered an event in the MPAWIN system. The data were recorded in a list file and processed off-line later. During the experiments all the

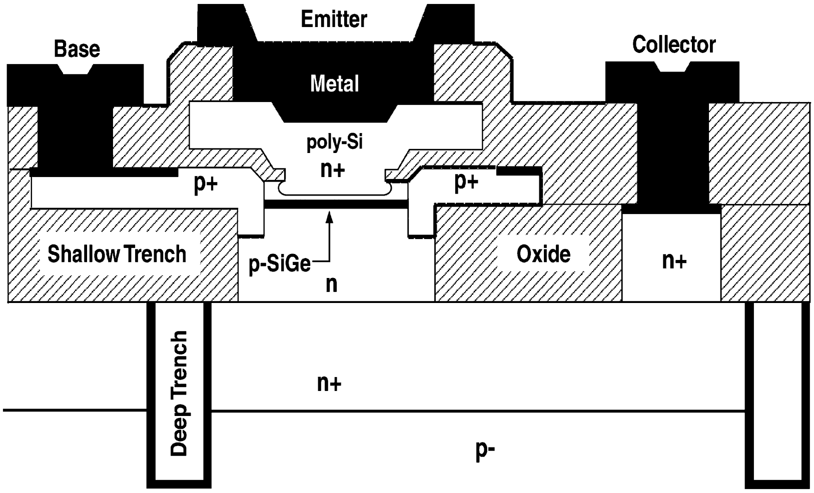

Fig. 1. Typical cross-section of a SiGe HBT after [1].