Available online at www.sciencedirect.com
ScienceDirect
Nuclear Instruments and Methods in Physics Research B 253 (2006) 250–254
NIM B
Beam Interactions with Materials & Atoms
www.elsevier.com/locate/nimb

2-D simulation and analysis of temperature effects on electrical parameters degradation of power RF LDMOS device

M.A. Belaïd *, K. Ketata, M. Gares, J. Marcon, K. Mourgues, M. Masmoudi

LEMI, University of Rouen, IUT Rouen, 76821 Mont Saint Aignan, France

Available online 1 November 2006

Abstract

This paper presents a synthesis of temperature effects on power RF Laterally Diffused (LD) MOS performances, which can modify and degrade transistor physical and electrical behaviour. In this work, the temperature influence on device electrical characteristics is discussed with regard to physical limits for device operation. A developed 2-D structure was implemented and simulated using the physical simulator Silvaco-Atlas to explain the observed data and offer insight into the physical origin of LDMOS temperature behaviour. The temperature dependence of most important electrical parameters such as channel current I_{ds}, threshold voltage V_{th} and inter-electrodes capacitances (C_{ds}, C_{gs}) is investigated. The temperature effects on mobility, electron concentration, electric field, current flow lines and Fermi level are taken into account. Finally, initial failure analysis is discussed.

Keywords: Simulation; Temperature effects; LDMOS; Interface defects

1. Introduction

In many applications of electronic, a growing demand for devices being capable of operating at increased temperatures is developing. The current tendency in microelectronic industry is to the down scaling of electronic components leading to power increase. This means that temperature effects must be taken into account both in the design as well as in the exploitation [1]. It is known that the temperature reached by the power device under operation exercises has a considerable influence on reliability and performances [1,2]. The temperature is one of the critical parameters in particular RF power electronic devices and many properties of these devices are strongly dependent on temperature.

The study of device parameters is important to he ensure reliable functioning, especially at a various temperature environment. The dependence of channel temperature change on device operation time is of special interest, as it represents the temperature distribution along the channel and throughout the basic chip. The increase of the temperature causes a change of silicon basic properties (band-gap, intrinsic carrier concentration, carrier lifetime and mobility, etc.) [3]. As a result, the basic electrical characteristics of power RF Laterally Diffused (LD) MOS transistors, such as channel current I_{ds}, threshold voltage V_{th} and inter-electrodes capacitances, are changed as well [4,5]. Our investigations are based on physics and 2-D simulations of the device; a new in-depth study of the temperature influence on the performances was mined.

2. Device experimental characterization and parameters extraction

It is essential to characterize RF LDMOS in order to extract model parameters. A commercial Philips RF LDMOS has been used for this study. The main characteristics of this device are as follows: frequencies up to 2 GHz, output power of 10 W, breakdown voltage of 75 V. I–V and C–V measurements were performed, respectively, by an Agilent E5270 DC analyser and HP 4194A impedance

* Corresponding author. Tel.: +33 2351 47179; fax: +33 2351 46254.
E-mail address: Mohamed-ali.belaid@univ-rouen.fr (M.A. Belaïd).

0168-583X/$ - see front matter © 2006 Elsevier B.V. All rights reserved.
doi:10.1016/j.nimb.2006.10.040

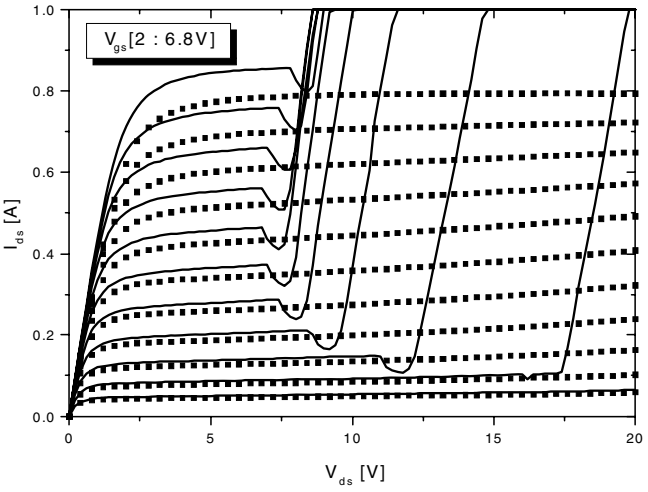

Fig. 1. Output characteristics: Thermal instability effect (line) and stable temperature conditions (dashed).

analyser, piloted by IC-CAP Agilent software. Special attention was paid to the fact that the RF LDMOS is a power device, so it heats up at high-bias. The method presented is based on a comparison of *I–V* and *C–V* characteristics of the transistor in various conditions (chip, package, heat sink, different temperatures) with the same component.

Fig. 1 (line) shows the instability and the thermal runaway which occurred due to self-heating effects. To limit this problem, a solution which proves to be a precious working tool would make it possible to stabilize the self-heating effects and to thermal protect the component. It consists of mounting the component on a heat dissipator (a heat sink or a Peltier module). Thanks to this solution, we can obtain more thermally stable measurement conditions (Fig. 1, dashed).

A new electro-thermal model is based on three cells representation (thermal network), from the chip to the ambient air, in order to fully describe the normal RF LDMOS *I–V* and *C–V* curves and to obtain a characterization able to evaluate the temperature variation and the self-heating effects during LDMOS operation. This model was used for power RF LDMOS devices as a tool to extract these parameters [2]. These results are compared and proved by a modified 2-D RF power N^- channel LDMOS structure previously developed by Raman et al. [6]; this structure has been implemented and simulated using the physical simulator Atlas of Silvaco [7]. The implemented structure is similar to our tested device. Consequently the qualitative understanding of physical phenomenon could be studied.

3. Results and discussion

In conventional MOS transistors, the highest current density is located in the channel region. Therefore, the most extensive power dissipation occurs in this region [1]. In addition, the rise of temperature is considerably larger when the device is operating in saturation, as a result of higher power dissipation than in the case of a device operating in the linear region [8]. Maximum temperature is observed in the channel pinch-off region because of maximum current density [8]. The *I–V* characteristics of the transistor in various conditions and the fitted results are in good agreement as shown in Fig. 2. Several levels of heat dissipation are presented which describes the temperature variations in the component.

These techniques also deal with the same phenomenon studied by Yang [9] in pulsed (long and short pulse) and in DC characterization. This explains the different means of component dissipation power, by using a cooling system is very essential in the case of DC characterization or exploiting pulse width to avoid heat rise in the case of pulsed characterization.

Knowledge of the temperature distribution inside the structure and in particular in the conduction channel and thus in the drift area, is necessary to identify local "hot spots" (Fig. 3).

However, the non-uniform distribution of dissipated power has been observed and is located in the drift region. It is caused by the breakdown effect and can lead to thermal runaway, if the rise in channel temperature is high-enough. As in other power devices, the temperature rise due to device self-heating takes place inside the LDMOS active area, thus degrading the static and dynamic electrical characteristics of the device and finally altering the performance to a considerable extent [10]. Besides the electro-thermal modelling improvement, accurate prediction of the temperature in the source/drain/channel is also desirable for a reliability study. Indeed, the failure rate depends on the temperature, as previously reported in [1,9].

The temperature rise increases the drain current due to the reduced threshold voltage at a low-current region and decreases it due to the effective mobility degradation at a high-current region [10].

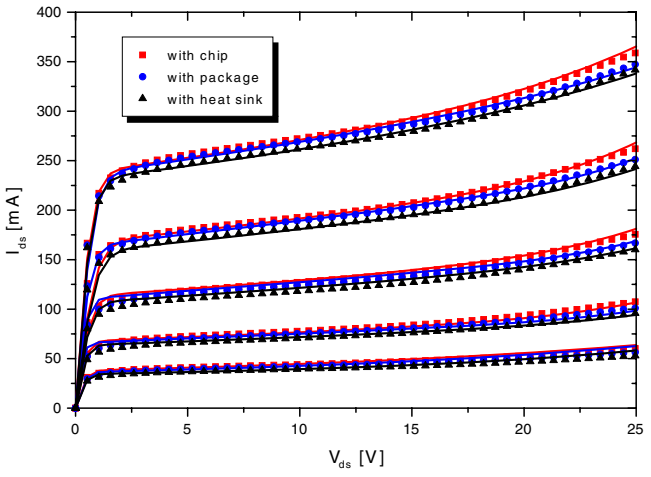

Fig. 2. Measured (dashed) and modelled (line) output characteristic under various measurement conditions, with V_{gs} = (3 V, 5.4 V), step = 600 mV.