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Grooving of grain boundaries in multicrystalline silicon: Effect on solar cell performance

W. Dimassi, M. Bouaïcha *, H. Nouri, M.F. Boujmil, S. Ben Nasrallah, B. Bessaïs

Laboratoire de Photovoltaïque et des Semi-conducteurs, Centre de Recherches et des Technologies de l'Energie, BP 95 Hammam-Lif, 2050, Tunisia

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Abstract

In this work, we investigate the effect of grooving of grain boundaries (GB) in multicrystalline silicon using chemical etching in HF/HNO_3 solutions. The grain boundaries were grooved in order to reduce the area of these highly recombining regions. Using optimized conditions, grooved GBs enable deep phosphorus diffusion and deep metallic contacts. As a result, the internal quantum efficiency (IQE), and the *I–V* characteristics under the dark and AM1.5 illumination were improved. It was also observed a reduction of the GB recombination velocity, which was deduced from light-beam-induced-current (LBIC) measurements. Such grooving in multicrystalline silicon enables passivation of GB-related defects. These results are discussed and compared to solar cells based on untreated multicrystalline silicon wafers.

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Keywords: Multicrystalline silicon; Chemical etching; Grain boundaries; Passivation; Gettering

1. Introduction

To increase the conversion efficiency of multicrystalline silicon solar cells, phosphorous (P) and aluminum (Al) gettering can be introduced in the cells fabrication process [1]. In order to improve the minority carrier diffusion length, long time P and Al gettering at high temperatures has been suggested [2]. A mixture of HF and HNO_3 and other acids is often used to etch the surface of multicrystalline and monocrystalline silicon substrates. The state of the etched surface depends on the proportion of the acids forming the mixture. A mixture of HNO_3:HF:CH_3COOH in the proportion 64%:16%:20% was used to give a fairly uniform surface without pronounced steps from grain to grain. HF/HNO_3-based solutions may also be used to obtain PS layers [3]. Another current use of HF/HNO_3 solutions is the isotropic texturing of mc-Si wafers [4]. A number of studies [5] have shown that chemical etching parameters such as etching time and the proportion of acids affect the solar cell performance. In a previous work [6], we reported an experimental approach to reduce the GB undesirable effects in multicrystalline silicon solar cells by introducing a porous silicon (PS) layer formed by a vapor etching (VE) based method [7]. This method consists of grooving GBs by forming a PS film. We observed that PS has a preferential formation at GB regions. We use this crucial property to groove the GBs. However, using this method, we encountered problems involved in stability and reproducibility of the PS films.

In this work, GBs were grooved using an alternative method consisting of immersing completely the multicrystalline silicon wafers into HF/HNO_3-based solution. The HF/HNO_3 volume ratio and the temperature were 4/1 and 25 °C respectively. This method enables further phosphorus (P) and Al diffusion along the GBs and enhances impurity segregation at both the front and back sides.

* Corresponding author. Tel.: +216 71 430 160; fax: +216 71 409 934.
E-mail address: Bouaicha.Mongi@inrst.rnrt.tn (M. Bouaïcha).

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2. Experimental details

Silicon solar cells were fabricated from 330 μm thick multicrystalline (mc-Si) p-type silicon wafers (boron-doped) having a resistivity in the range of 0.5–2.0 Ω cm, and a surface area of 4 cm^2 (2 cm × 2 cm). We chose identical samples (i.e. they have the same distribution of grains and GBs). For this purpose, we cut identical samples (2 cm × 2 cm) in identical mc-Si wafers. The latter were chosen with a great care to ensure that they are cut successively in the same ingot.

Two sets of solar cells (RSC: Reference Solar Cell and GSC: Grooved Solar Cell) were used in this work. The RSC were fabricated using an ungrooved wafer. The base mc-Si material of the RSC were subjected to a front and back etching using a HNO_3:HF:CH_3COOH solution in the proportion 64%:16%:20% (CP4 solution) at 25 °C and without any activation. Such an etching removed 10–20 μm of the surface and subsurface saw damage. The GSCs were fabricated using a grooved mc-Si wafer. For this wafer, front and back grooves were achieved using a mixture of HF (40%) and HNO_3 (75%) for an optimized period of 30 s. The HF/HNO_3 volume ratio and the temperature of the solution were fixed to 4/1 and 25 °C, respectively. Using gravimetric measurements, we estimated the removed thickness during the etching procedure to be in the range of 15–20 μm. Hence, both RSCs and GSCs were fabricated using wafers having approximately the same thickness.

When the wafers were ready, P diffusion was performed at 925 °C during 20 min in a quartz tube furnace. The screen printed Al and Ag back and front metallic contacts were fired at 550 and 850 °C, respectively.

3. Surface characterization

Fig. 1(a) shows a scanning electron microscopy (SEM) surface image of an untreated multicrystalline wafer. This image is focused on two grains separated by a GB. After the HF/HNO_3 treatment, we notice a removal of the saw damage together with a significant grooving of the GB (Fig. 1(b)). From the cross section SEM view of the grooved GB (Fig. 1(c)), we may estimate a grooving depth of about 12 μm as compared to the lateral grain surface level.

As compared to the untreated multicrystalline wafer (Fig. 1(a)), and in spite of the apparent changes in the surface morphologies after etching (Fig. 1(b) and (c)), it is

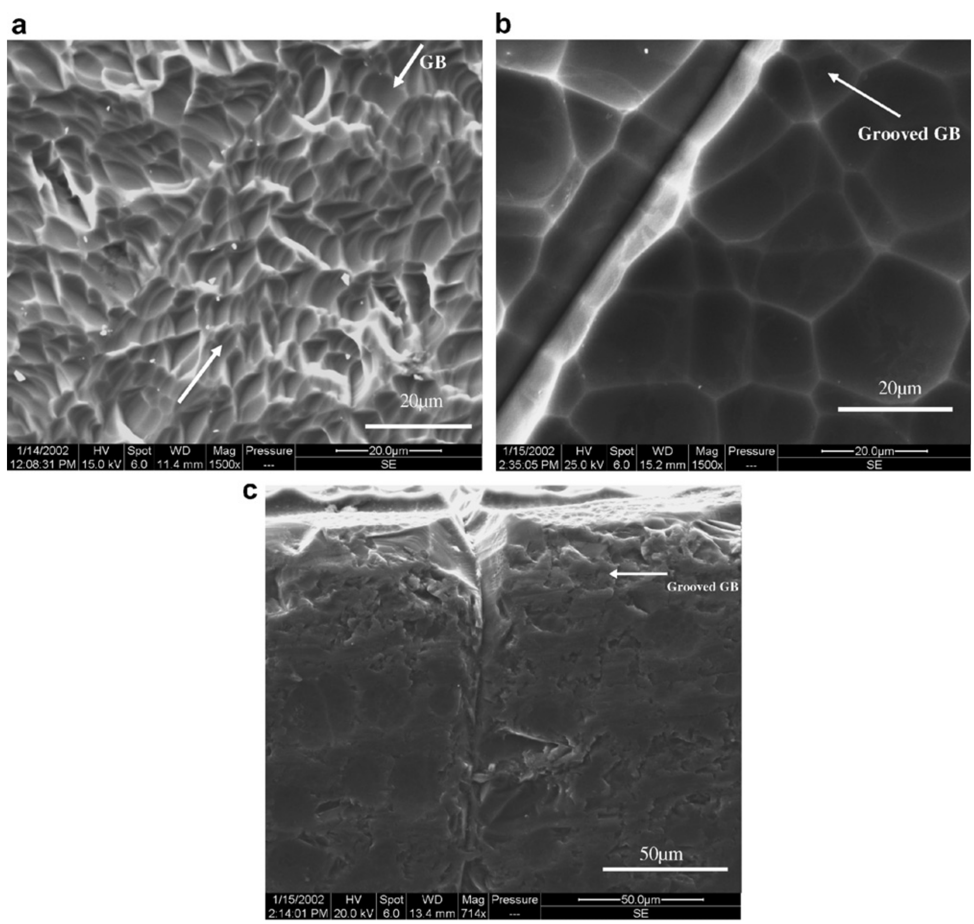

Fig. 1. (a) SEM surface image view of an untreated mc-Si wafer showing the ungrooved GB. (b) Typical SEM top view of a HF/HNO_3 treated mc-Si wafer showing a grooved GB. (c) Cross section SEM view of a grooved GB.