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Invited review

Device applications of epitaxial graphene on silicon carbide

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ABSTRACT

Graphene has become an extremely hot topic due to its intriguing material properties allowing for ground-breaking fundamental research and applications. It is one of the fastest developing materials during the last several years. This progress is also driven by the diversity of fabrication methods for graphene of different specific properties, size, quantity and cost. Graphene grown on SiC is of particular interest due to the possibility to avoid transferring of free standing graphene to a desired substrate while having a large area SiC (semi-insulating or conducting) substrate ready for device processing. Here, we present a review of the major current explorations of graphene on SiC in electronic devices, such as field effect transistors (FET), radio frequency (RF) transistors, integrated circuits (IC), and sensors. The successful role of graphene in the metrology sector is also addressed. Typical examples of graphene on SiC implementations are illustrated and the drawbacks and promises are critically analyzed.
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Contents

1. Introduction

Graphene is a sp^2 bonded sheet of carbon atoms with honeycomb symmetry that shows non-dispersive transport characteristics. In graphene, electrons move as relativistic Dirac particles with a velocity ~10× higher than in a conventional semiconductor. Carrier mobilities more than 100 000 $cm^2/V \cdot s$ [1,2] and saturation velocities of about 5×10^7 $cm^{-2}s^{-1}$ have been reported [3]. These properties in addition to a high current density up to 10^9 A/cm^2 and high thermal conductivity up to 5000 $W\ m^{-1}\ K^{-1}$ [4] make it extremely appealing for applications in electronics. The two-dimensional nature of graphene enables tight control of the carrier density using the field effect [5], and permits the use of conventional semiconductor processing techniques.

It is worth noting that most of these extraordinary properties are related to pristine graphene [6] under slightly idealized conditions such as graphene exfoliated from highly oriented pyrolitic graphite (HOPG), suspending the sheets between metal leads, or using an ultra flat and inert substrate as BN. In research and

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technology, graphene is used in more complex structures, and at conditions that are determined by the targeted applications. For instance, electrical transport is subject to a variety of scattering events [7–12]. The type of scattering mechanism that dominates in a specific sample could be derived from the magnitude of the carrier mobility (μ), and its dependence on temperature (T) and carrier density (n) [13]. Therefore, mobilities greater than 100 000 $cm^2/V \cdot s$ are known to indicate scattering that is dominated by acoustic phonons, where $\mu_{AC} \sim 1/n$ [1,2,9]. This is typical for graphene when the substrate is removed and it is heated in order for the adsorbates to volatilize. Long-range Coulomb scattering results in mobilities of the order of 1000–10 000 $cm^2/V \cdot s$ that are independent of carrier density, n [8,10,11]. It is related with charge impurities on graphene or more likely at the supporting insulator substrate. Neutral defects become significant in either highly defective samples or at high carrier densities and mobility dominated by short-range scatter, $\mu_{SR} \sim 1/n$ [7,11,14,15].

In most of the electronic applications graphene is supported by a dielectric substrate (typically SiO_2 or high-k dielectrics) or by semi-insulating SiC. In this cases the values of the electron mean free path l_{gr} and mobility observed in supported graphene are usually significantly lower than in a suspended one. Sonde at al [16] studied the local l_{gr} in graphene deposited on 4H–SiC (DG-SiC) i.e (graphene exfoliated from highly oriented pyrolitic graphite (HOPG) and deposited on 4H–SiC(0001)), graphene epitaxially grown on 4H–SiC(0001) (EG-SiC) and graphene deposited on SiO_2 (DG-SiO_2), by scanning capacitance spectroscopy. The electron mean free path in DG-SiC was more than four times longer than in DG-SiO_2. This difference can be related to the difference in the permittivity of SiC ($\varepsilon_{SiC} = 9.7$) and SiO_2 ($\varepsilon_{SiO_2} = 3.9$), and respectively to the lower coupling of the 2DEG (two-dimensional electron-gas) with SPP (surface polar phonons) in SiC than in SiO_2. On the other hand l_{gr} in EG-SiC is on the average 37% of the l_{gr} in DG-SiC and exhibits large variations from point to point, due to presence of a laterally inhomogeneous positively charged layer at the EG/SiC interface.

Giannazzo et al. [17] used a method based on scanning capacitance microscopy/spectroscopy to obtain 2D maps of the electron free path (l) in graphene obtained by mechanical exfoliation of highly oriented pyrolitic graphite (HOPG) and deposited on substrates with different dielectric permittivity, that is, SiO_2 ($k_{SiO_2} = 3.9$), 4H–SiC(0001) ($k_{SiC} = 9.7$) and the very-high-k perovskite strontium titanate, $SrTiO_3$(001), referred to briefly as STO ($k_{STO} = 330$). Such maps are a powerful instrument to understand the scattering mechanisms such as charge impurities (CI) and resonant scattering (RS) limiting the transport properties in graphene at room temperature. CI can be adsorbed on graphene, or located at the graphene/substrate interface while, according to the density functional theory calculation, RS in graphene occurs naturally for vacancies, and adsorbates like H, OH and CH_3, CH_2OH [18]. It was shown that CI are the main source of the lateral inhomogeneity of l in graphene on low-k substrates, while the role of RS as a limiting factor for l was more pronounced in graphene on high-k STO.

For high performance applications mobility maximization and uniformity are required at the wafer scale, therefore techniques producing graphene with unique azimuthal orientations over a whole wafer are needed. In the following we discuss graphene materials grown on SiC which meets the above requirements.

The graphitization of hexagonal SiC crystals during annealing at high temperature in vacuum was reported by Badami DV as early as 1962 [19]. Under such annealing conditions the top layers of SiC crystals undergo thermal decomposition. Since Si has the highest partial vapor pressure, Si leaves the surface while C nominally remains on the surface, rearranges and re-bonds to form epitaxial graphene layers possessing in-plane sp^2 bonding [20–22].

Graphene formation occurs in a top-down manner starting by decomposition of the SiC substrate surface and proceeding into the SiC bulk [23,24]. Decomposition of about three Si–C bilayers (~0.75 nm) is required in order to arrange one graphene layer (~0.34 nm). On the Si face of SiC, initially a C-rich $(6\sqrt{3} \times 6\sqrt{3})$ R30° surface reconstruction occurs, which is known as a buffer layer or zero graphene layer [25]. In such layers the C atoms are arranged in a similar honeycomb structure to graphene, but there is 30% covalent bonding to underlying Si atoms [17]. Thus the buffer layer provides a template for subsequent epitaxial growth. It has been debated whether growth of graphene on SiC is really epitaxial under conditions of a large lattice mismatch between SiC (3.073 Å) and graphene (2.46 Å) as the carbon self-rearranges on the SiC substrate surface rather than being deposited on the SiC surface, as would arise in a classical epitaxial growth [26]. However, it has to be noticed that growth of graphene on SiC by Si sublimation does not occur on a pristine SiC surface, but is mediated by the C-rich reconstructed surface which, due to its structural compatibility with grapheme, appears to be a perfect template for graphene formation in an ordered manner, i.e. epitaxially.

In terms of electrical properties, the buffer layer is not equivalent to graphene. This layer is not conducting and does not bear the electronic properties of graphene because of the sp^3 bonding to the SiC substrate. The buffer layer is responsible for the n-type doping of pristine graphene on SiC (0001) due to the presence of unsaturated Si bonds.

In the course of graphene growth a new buffer layer forms below the first one that is simultaneously converted to graphene. A second graphene layer can grow in the same manner. It is more difficult to grow multilayer graphene on SiC [27] due to the decreased Si desorption rate from the buried SiC decomposition front. Si removal in this case occurs via diffusion through defects in graphene (mainly terrace edges) and/or the sample edge. More graphene layers form when pronounced defects, like polishing scratches and micro-pipes, are present on the substrate surface.

It has been shown that the graphene on Si-face SiC grown at high temperature, 2000 °C, possesses superior properties such as structural integrity and uniformity of graphene over hundreds of micrometers, as well as reproducible mobility and carrier concentrations across a half-centimeter wafer, which allowed precise measurements of quantum Hall resistance [28].

On the other hand, on the C face of SiC the first graphitic layer grows on top of the SiC substrate without causing a strong rearrangement of the surface structure. There are still debates about the structure of the interface layer, i.e. whether graphene growth on the C face is preceded by ordered surface reconstructions [29] or a disordered/amorphous interface layer [30].

Low bias STM (scanning tunneling microscopy) images revealed a graphitic structure, indicating that the interaction between graphene and the SiC surface is weaker on the C face than on the Si face of the SiC substrate [29].

Coby et al. [30] report formation of an amorphous layer at the interface of graphene films grown via thermal decomposition of C-face 4H–SiC at 1600 °C. Electron energy loss spectroscopy (EELS) demonstrates that the amorphous layer is carbon-rich. Few-layer graphene films grown under similar conditions on Si-face substrate were not observed to contain any such amorphous layer [31].

Nicorta et al. [32] show that for high growth temperatures like 1900 °C the graphene/SiC $(000\bar{1})$ interface is dominated by a thin amorphous film which strongly suppresses the epitaxy of graphene on the SiC substrate, since its thickness ~1.1–1.4 nm is bigger than the range of chemical bonds between atoms of the first graphene layer and the last SiC bilayer. This film maintains an almost fixed thickness regardless of the number of the overlying graphene layers. High-resolution EELS shows the presence of C, Si and O.

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