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Deposition and characterization of ultra-high barrier coatings for flexible electronic applications

Tsai-Ning Chen [a], Dong-Sing Wuu [a,*], Chia-Cheng Wu [a], Ray-Hua Horng [b], Hsiao-Fen Wei [c], Liang-You Jiang [c], Hung-Uang Lee [c], Yu-Yang Chang [c]

[a] Department of Materials Science and Engineering, National Chung Hsing University, 250 Kuo Kuang Rd., Taichung 40227, Taiwan, R.O.C.
[b] Institute of Precision Engineering, National Chung Hsing University, Taichung 40227, Taiwan, R.O.C.
[c] Display Technology Center, Industrial Technology Research Institute, Hsinchu 31040, Taiwan, R.O.C.

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A barrier structure consisting of SiO_x and SiN_x films was deposited on the polymer substrate at 80 °C via plasma-enhanced chemical vapor deposition (PECVD). However, the low radius of curvature (R_c) of the barrier-coated substrate may cause the inconvenience of the following fabrication processes. By depositing a 150 nm-SiN_x film, the R_c of the barrier-coated polycarbonate (PC) substrate can increase from 80 to 115 mm without inducing any cracks in the barrier structure. Furthermore, the thermal stress of the barrier structure can be adjusted via extending the PECVD process duration in the chamber and replacing PC by the polyethersulone (PES) substrate. The R_c can increase to ∼356 mm by depositing the 150 nm-SiN_x film on the other side of the PES substrate. Finally, the calcium test result of the barrier films/PES/SiN_x sample was calculated to be around 3.05×10^{-6} g/m^2/day, representing that the barrier structure did not fail after modification.

1. Introduction

Barrier coatings have been investigated intensively for the passivation of organic solar cells and organic light emitting diodes (OLEDs) [1]. The promise of these organic electronics lies in the potential for building large area electronic devices with lower cost than possible with conventional silicon-based technology [2]. To fulfill these low-cost electronic technologies, flexible substrates are used to replace glass substrates. Nevertheless, the properties of polymers often do not meet the demands regarding scratch-resistance, against photo-degradation and gas permeation. Therefore, the combination of polymer materials with functional barrier coatings is used to solve these problems [3]. For a long time, how to effectively encapsulate the device layers from the ingression of water vapor and oxygen is regarded as the major subject. Many researchers have devoted to achieve this goal with the water vapor transmission rate (WVTR) and the oxygen transmission rate (OTR) of the barrier films $<10^{-6}$ g/m^2/day and $<10^{-3}$ cm^3/m^2/day for OLEDs, respectively [4]. Pacific Northwest National Laboratory, Universal Display Corporation and Vitex Systems Inc. have all demonstrated an organic–inorganic multilayered barrier film with promising moisture permeation rates in the range of 10^{-6}–10^{-5} g/m^2/day [4,5]. However, seldom groups have discussed the stress resistance and the curvature of these ultra-high barrier structures. In this paper, we tried to increase the radius of curvature (R_c) of the barrier structure by depositing a SiN_x film at the other side of the polymer substrate. SiN_x films with different compressive stresses were applied to provide different tensile stresses on the barrier structures. Polyethersulfone (PES) substrates were used to replace the polycarbonate (PC) substrate because of lower coefficient of thermal expansion (CTE).

2. Experimental

SiN_x and SiO_x films were deposited on polymer substrates by plasma-enhanced chemical vapor deposition (PECVD) at 80 °C. Deposition parameters of SiN_x films were SiH_4/NH_3 flow rate 130/20 sccm, RF power 100–150 W, and pressure 800 mTorr; deposition parameters of SiO_x films were SiH_4/N_2O flow rate 150/100 sccm, RF power 30–80 W, and pressure 800 mTorr. The molded PC substrates were 178 μm in thickness with a glass-transition temperature (T_g) of ∼140 °C and the PES substrates were 200 μm in thickness with a T_g of ∼220 °C. The three-dimensional (3-D) image and surface roughness were analyzed using a Wyko NT1100 (Veeco) optical profiler. Optical microscopy was used to observe the fragmentation patterns on the barrier films. The film stress of the

* Corresponding author. Fax: +886 4 22855046.
E-mail address: dsw@dragon.nchu.edu.tw (D.-S. Wuu).

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SiN_x coatings on Si wafers was determined using a Tencor FLX-2320 laser profilometer. A calcium test was used to calculate the WVTR of the ultra high barrier structure on polymer substrates. By observing the percentage of color changing area, one could calculate WVTR values effectively.

3. Results and discussion

Ultra-high barrier structure with a WVTR value $\sim 10^{-6}$ g/m^2/day calculated by Ca test at 25 °C, 40% RH was achieved in our previous study [6]. However, the total stress of the barrier structure is very high. As shown in Fig. 1(a), the 3-D image of the barrier-coated PC substrate demonstrates a low $R_c \sim 76$ mm. The curvature induced by the compressive internal stress of the barrier films may cause inconvenience of the following procedures and the design of the devices. The aim of this paper is to improve the flatness of the barrier-coated substrate. First of all, we decided to deposit the same barrier structure on both sides of the PC. The both sides of PC were coated with six pairs of SiO_x/SiN_x stacks capped with a SiN_x film on the top. It was of the opinion that the same internal stress of the barrier films might counteract the curvature theoretically. Nevertheless, the barrier films turned out to crack after the same barrier structure was deposited on the back side of PC. As shown in Fig. 1(b), the optical microscopy image of the barrier structure demonstrates a delamination. Fragmentation was found to start at the edge of the sample due to the strength and defect distribution of the barrier coating [7]. Finally, the substrate became flat because the stress relaxation occurred during the fragmentation process. It was found that depositing the same barrier structure on the back side will cause the main barrier structure to lose its efficiency.

To deposit a barrier film with adequate stress on the back side, the stresses of SiN_x coatings with different film thicknesses were illustrated in Fig. 2(a). The stress of the SiN_x films deposited under RF power 150 W becomes more compressive with increasing film thickness from 50 to 200 nm. It was found that the stress of a 250 nm-SiN_x film on Si wafer becomes less compressive because of the formation of cracks [8]. Since the coherence between polymer and SiN_x is less than Si and SiN_x, we chose to deposit SiN_x coatings with film thickness from 50 to 200 nm on the back side of the PC for further investigation. As shown in Fig. 2(b), the R_c of the barrier-coated substrates increase from 80 to 135 mm without and with the deposition of SiN_x film. With the increasing film thickness of the SiN_x on the back side of PC, the R_c increases correspondingly. Each R_c demonstrated here is the average value obtained from three different samples. It was observed that the main barrier structure failed after depositing a 200 nm-SiN_x film (not shown). Once again, cracks started to generate at the peripheral of the optimum barrier structure. Therefore, the barrier structure cannot withstand the tensile stress provided by the 200 nm-SiN_x film. The acceptable largest film thickness of SiN_x on PC/barrier structure is around 150 nm and the radius R_c can be enhanced to 119 mm without a specific crack generation.

Besides depositing a SiN_x film on the back side, reducing the thermal stress of the optimum barrier films is used for further

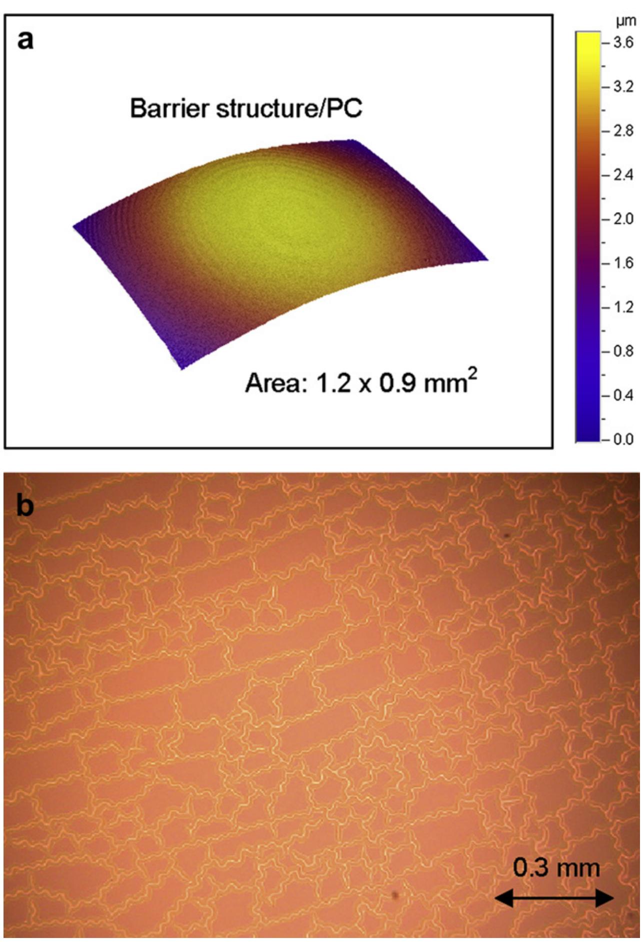

Fig. 1. (a) 3-D image of the ultra-high barrier structure on PC substrate. (b) Fragmentation patterns on the surface of the double-side coated PC substrate.

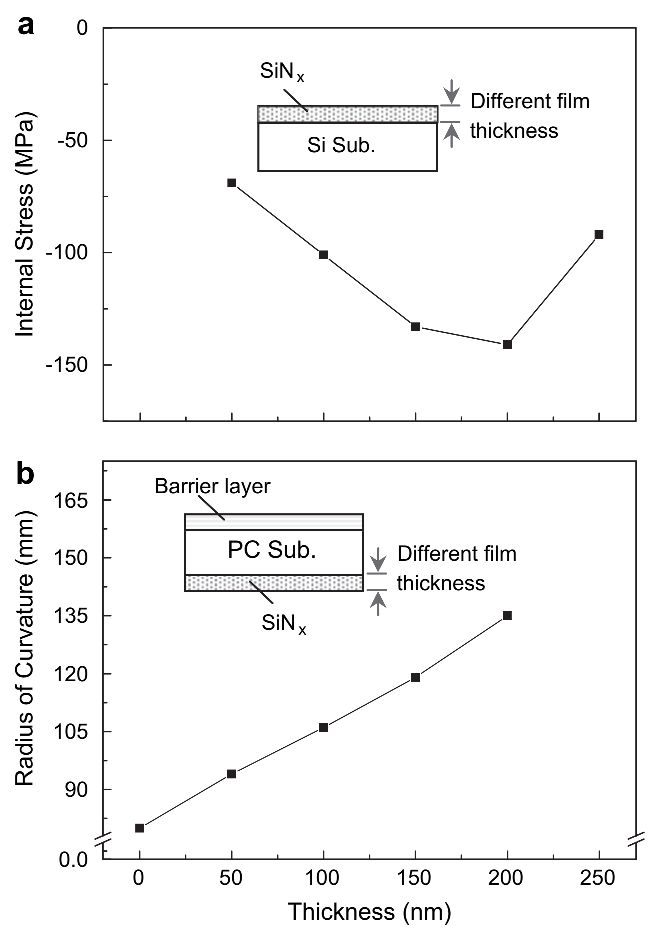

Fig. 2. (a) Internal stress of SiN_x films deposited at RF power 150 W on 4″ Si wafers as a function of film thickness. (b) Radius of curvature of the double-side coated PC substrate as a function of different SiN_x film thickness.