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Numerical simulation of bias and photo stress on indium–gallium–zinc-oxide thin film transistors

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ABSTRACT

Thin Film Transistors based on amorphous Indium–Gallium–Zinc-Oxide (a-IGZO TFT) are receiving a great deal of attention for their numerous applications as alternatives for amorphous and poly-crystalline Silicon based TFTs. A major concern about a-IGZO TFTs is that they suffer from instabilities when subjected to different types of stress (bias, light, etc …). Stress is believed to create defects of different kinds in different regions of the device. The instability manifests as a shift in the threshold voltage or a hump in the transfer characteristics of the transistor. In addition, there is still a great deal of confusion about the relation between defects and the instability induced by stress. The main purpose of this study is to elucidate the relation between the threshold voltage shift (instability) and the defects created by stress. For this purpose a detailed numerical simulation was carried out to investigate the relation between the different types of defects created by stress and the induced instability in a-IGZO TFT. It was found that tail, deep and interface states cause a shift in threshold voltage. Negative and positive shifts are observed if the defects are donor-like and acceptor-like defects, respectively. On the other hand, a hump in the transfer characteristics is induced if discrete interface levels are dominant.

1. Introduction

Thin film transistors (TFTs) are used in numerous electronics applications such as active matrix organic light emitting diodes (AMOLED), active matrix liquid crystal display (AMLCD) [1,2], and fast circuits [3]. Although several materials such as amorphous silicon (a-Si), polycrystalline silicon (pc-Si) and organic semiconductors (OS) can be used as active layers for TFTs, there has been growing interest in amorphous oxide semiconductors (AOS) based on zinc oxide (ZnO) such as indium–gallium–zinc oxide (IGZO) [4]. a-Si and OS TFTs have a low field-effect mobility while pc-Si TFTs suffer from non-uniformity over large areas [5]. IGZO TFTs have several advantages which include visible light transparency [6], large-area uniform deposition at low temperature [7], good controllability of carrier concentration [5] and high carrier mobility [8]. However, the threshold voltage of a-IGZO TFTs, like in other TFTs, can be severely degraded by different types of stress such as negative or positive bias, temperature, exposure to light or even mechanical strain [9,10]. This phenomenon is referred to as threshold voltage instability. It is believed that stress induced instability is due to defects created in different regions of the device. Lopes et al. [11] reported that the origin of the threshold voltage instability is due to the change trapping at residual-water-related trap sites following a gate voltage stress. Liu et al. [12] related the shift in the electrical characteristics after a negative gate bias (NGBS) prolonged stress to the degradation of the contact between source/drain and a-IGZO active layer. The distribution of states in the conduction band can also be affected by a prolonged bias stress [13]. Light stress also induces threshold shift [14] which is related to the capture of photo-induced hole carriers by donor-like interface traps. Dao et al. [15] related the threshold instability to carrier trapping rather than defect creation after the device was subjected to a prolonged gate bias stress. A hump may also appear in the electrical characteristics of a-IGZO TFTs subjected to a large positive gate bias stress [16]. Deep states above the valence band, created by constant current stress and negative bias stress at the surface of a-IGZO under illumination, may also be responsible for the instability [17]. The degradation mechanism of a-IGZO TFTs

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under positive gate bias and negative gate bias with illumination are attributed to electron and hole trapping, respectively, at the insulator-channel interface [18]. The exposure of an a-IGZO TFT to ultraviolet radiation induces a negative shift in its electrical characteristics despite that no bias stress is applied [19]. This shift is explained by the ionization of neutral oxygen vacancies in the active layer. It was also observed that negative bias enhances the shift while positive bias reduces it. Jeon et al. [20] found that illuminated a-IGZO TFTs showed stable characteristics under positive gate bias stress but a huge shift in the threshold voltage under negative gate bias stress. In this case it is believed that hole trapping in the gate dielectric layer is the major cause of this degradation. In order to elucidate the difference between bias and illumination stress, Vemuri et al. [21] showed that excessive positive gate bias stress creates charge trap states while light with wavelengths below 532 nm create ionised vacancies. Although there were several attempts to reduce instability following different types of stress such as temperature annealing, addition of a buffer layer, and chemical treatment, the phenomenon still persists.

It is therefore evident that there are a lot of non-clarified issues related to the effect of different means of stress on the electrical characteristics of a-IGZO TFTs. In particular what kind of stress (optical, gate bias, drain bias, temperature, etc.) creates which of defects (interface, bulk, discrete levels, continuous DOS, etc).

This work is an attempt to investigate a specific side of this issue. In particular it will be assumed that a stress, whatever its nature is, will create either an interface defect between the active channel (a-IGZO thin film) and the dielectric material, a bulk defect in the active channel (as a Gaussian acceptor or increase the initial Gaussian donor) or a bulk defect in the dielectric. The transfer characteristics of the a-IGZO TFT under these different assumptions are numerically calculated using the SILVACO TCAD software [22]. Numerical simulation has the unique feature that the effect of different parameters can be studied independently or simultaneously. This, obviously, cannot be achieved by experimental work or analytical modelling.

2. The a-IGZO TFT structure

A two dimensional cross-section along the channel of the a-IGZO TFT structure used in this work is shown in Fig. 1 which is a staggered bottom-gate similar to that of reference [23]. The channel is 20 nm thick a-IGZO, the substrate is a heavily doped n-type poly-silicon which also acts as a gate, the gate insulator is a 100 nm thick SiO_2 layer, the drain and source Ohmic contacts are 5 μm long low resistance titanium (Ti). The separation between the source and drain is 30 μm.

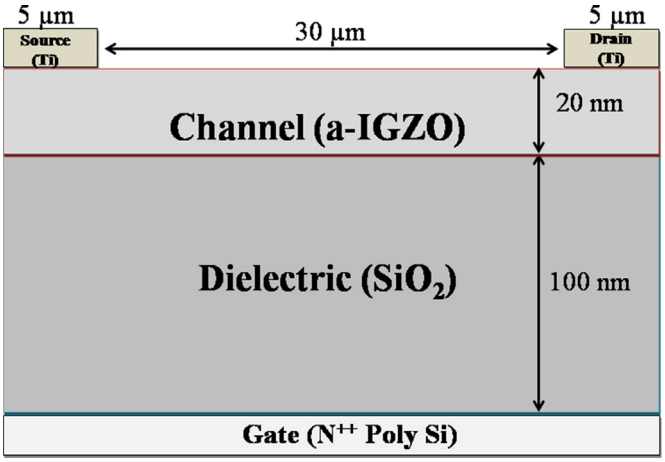

Fig. 1. A two dimensional view of the a-IGZO TFT structure simulated in this work [24].

The channel is made of a-IGZO which is an amorphous n-type semiconductor. Its structural properties are adapted from those of amorphous hydrogenated silicon (a-Si:H) [24]. Disordered materials (like a-Si and a-IGZO) contain a large number of defect states continuously distributed within the band-gap of the material. The density of states is a combination of exponentially decaying band tail states and Gaussian distributions of mid-gap states.

The conduction band-tail (CB) states (acceptor-like states $g_{ct}^{A}(E)$) are givin by exponential function decay:

$$g_{ct}^{A}(E) = g_{ta}\exp\left(\frac{E - E_C}{E_a}\right)$$

where $g_{ta}(cm^{-3}\ eV^{-1})$ is the effective density at E_C, and E_a is the characteristic slope energy of the conduction band-tail states.

The valence band-tail (VB) states (donor-like states $g_{vt}^{D}(E)$) are also given by a similar expression:

$$g_{vt}^{D}(E) = g_{td}\exp\left(\frac{E_V - E}{E_d}\right)$$

where $g_{td}(cm^{-3}\ eV^{-1})$ is the effective density at E_V, and E_d is the characteristic slope energy of the valence band-tail states.

In addition to tail states, Gaussian-distributed donor-like and acceptor-like defect states, $g_G^D(E)$ and $g_G^A(E)$, respectively, in the energy gap are also considered

$$g_G^D(E) = g_{gd}\ \exp\left(-\frac{(E - E_D)^2}{\sigma_D^2}\right)$$

$$g_G^A(E) = g_{ga}\ \exp\left(-\frac{(E_A - E)^2}{\sigma_A^2}\right)$$

where g_{gd} (g_{ga}), are the total density ($cm^{-3}\ eV^{-1}$), σ_D (σ_A) the standard deviation and E_D (E_A) the peak energy of the Gaussian distribution. The schematic DOS in amorphous semiconductors is shown in Fig. 2.

For a-IGZO, the conduction band minimum (CBM) is mainly made of the empty s orbitals of the metal cation and the valence band maximum (VBM) is of fully occupied O-2p orbitals [25]. CBMs of oxides are made of spherically spread s orbitals of metal cations, and their overlaps with neighbouring metal s orbitals are not altered largely by disordered amorphous structures. Therefore, electronic levels of CBM are less sensitive to local strained bonds [26], while, the O-2p orbital have various directions in amorphous oxides due to the disorder of the amorphous structure. This accounts for the origin of the p orbital localization and the valence band tail states. In addition, this explains the reason why the VB tail states have a wider distribution compared to the CB tail states which are very narrow [27].

The energy levels of oxygen vacancies (VO), that is, the non-bonding state of the metal cation, is formed in or near the CBM allowing the vacancies to act as a shallow donor but not as an effective electron trap. It should be noted that such donor states are not stable in many oxides. Even in such cases, the oxygen vacancy level is relaxed to form a fully occupied deep state, which no longer traps an electron and is inactive for electron transport in n-channel TFTs [28,29]. These deep states explain why a-IGZO TFTs do not show an inversion operation because the high-density occupied