Vacuum 84 (2010) 224–227

Contents lists available at ScienceDirect

Vacuum

journal homepage: www.elsevier.com/locate/vacuum

Characterization of sputter deposited Au/Ni/Al multilayers on Si substrates

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Keywords:
Au/Ni/Al multilayer structure
AES depth profiling
Thermal annealing

ABSTRACT

Multilayered Au/Ni/Al thin film metallization deposited by DC sputtering on n^+Si substrates has been investigated. AES depth profiling was performed to reveal the concentration depth profiles of the Au/Ni/Al multilayers before and after annealing at different temperatures in the range 623–723 K. It was found that Ni aluminide layers begin to form during heat treatments at temperatures above 623 K. In addition to this process, Ni was found to diffuse significantly through the Au layer and segregates at the surface, proportionally to the increased annealing temperature. Consequently, the Ni oxidation process was found to take place thus causing the degradation of electrical contact. On the other hand Ni diffuses faster as well toward the Si/Al interface. No contamination traces at interfaces were observed. Electrical measurements of the metallized diode forward characteristics showed minor influence of the metallization heat treatment on the series resistance. Degradations were observed only in the reverse characteristics if the annealing was performed above 723 K.

1. Introduction

Sputter deposition of metal thin films is widely used in the fabrication of various microelectronic and microelectromechanical devices. Proper material selection, deposition methods and thermal treatments are essential in achieving requirements such as long-term stability, solderability or compatibility with various epoxy-based conductive glues and low series resistance. Beside the low ohmic contact to enable good electrical functional performances, strong adhesion of metal thin films to silicon is mandatory to avoid delamination during bonding and packaging.

A single metal layer or a stack of metal layers is required to form a good ohmic contact between the silicon device and the external terminals. For efficient collection of light-generated carriers throughout the vertical structure of photosensitive p+nn+ device as shown in Fig. 1, electrical contacts are placed on the front and on the rear side of the device. Due to these metallization requirements the metallization scheme in our case comprises front side Al sputtered metallization pads and a backside solderable Au/Ni/Al sputtered metal stack. The choice of metals is very similar to that used in the flip chip technology; however, deposition processes are different [1]. For the backside metallization, the Al layer provides both an adherent bond to the silicon surface and a diffusion barrier preventing intermixing of Si and Ni. Ni provides a surface which is convenient for soldering, while Au serves as a Ni protection and a wetting layer appropriate for silver epoxy die attachment or soldering.

In this paper the properties of DC sputtered Au/Ni/Al multilayer backside metallization scheme on Si substrate such as interface structure, the adhesion and series resistance of metallized p^+nn^+ structure were characterized and investigated with respect to different thermal annealing treatments performed in the range 623–723 K. The main objective of this investigation was to determine the potential influence of thermal treatment, which might affect the mechanical or electrical properties of the final device after the completed fabrication, assembly and final testing.

2. Experimental methods

Experimental work was carried out on 100 mm diameter, high resistivity (500 Ωcm), n-type, one side mechanically polished float zone (FZ) silicon wafers with <100> crystal orientation. The metallization process was carried out with MRC603-I sputtering equipment as the last step in fabrication of the device under investigation. The background vacuum of the sputtering system was maintained at 2.7×10^{-5} Pa. The Ni was sputtered from a planar target with declared purity of 99.95%. The other two targets were planar Au target with purity of 99.7% and an inset Al target with purity 99.99%, respectively. The standard sputtered backside metallic stack applied in our p^+nn^+ photosensitive device consisted of Au (200 nm)/Ni (350 nm)/Al (750 nm). The thickness

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doi:10.1016/j.vacuum.2009.04.067

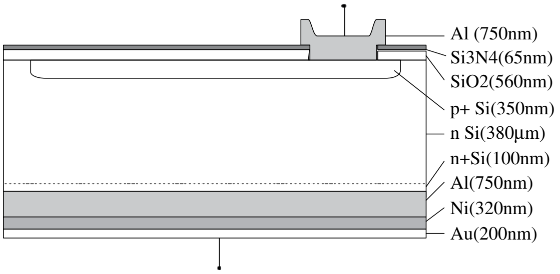

Fig. 1. Schematic cross-section of the metallized device structure.

of individual metal layers was measured by a Taylor Hobson surface profilometer.

Thermal annealing of metallized wafers was performed in a forming gas (5% H_2:95% N_2) atmosphere in quartz tube. The annealing time for all the samples was 30 min.

Auger electron spectroscopy (AES) depth profiling of Au/Ni/Al multilayers was performed in the PHI SAM 545 spectrometer. For electron excitation a primary electron beam of 3 keV and 2.6 μA, with a diameter of 40 μm, was used. During depth profiling the samples were sputtered by two symmetrically inclined 1 keV Ar ion beams at an ion incidence angle of 47° with respect to the surface normal. The atomic concentrations were calculated by means of relative sensitivity factors given by the instrument manufacturer [2].

For the qualitative adhesion strength a scotch tape pull test was applied on diced samples of equal size ($3 \times 5\ \text{mm}^2$).

Electrical characteristics and device properties such as forward and reverse *I–V* dependences were measured by a semiconductor parametric analyzer HP4155A. From these characteristics, the influence of the annealing process on the electrical properties such as the increase of leakage current and the change in series resistance, respectively, was determined.

3. Results and discussion

After performing the complete wafer processing, the metallization process steps were applied. Aluminium sputter deposition is first performed on the front side of the wafer where active p+n photosensitive diodes are fabricated. To obtain a hydrophobic silicon surface in contact pads, a short chemical treatment is performed prior to metal deposition. A 3 min treatment in 49% HF:DI water (1:100) followed by DI (de-ionised) water rinse and N_2 drying was used prior to each sputtering process. Front Al pads were then selectively etched by a photolithographic process. In the next step, aluminium is deposited also on the backside of the entire wafer by applying the same procedure as described above.

The requirements for electrical connections of the device usually employ Au wire bonding of the front contact. On the front side, the native Al_2O_3 barrier, which forms on the Al pad, is easily penetrated during the wire bonding process which is usually performed by ultrasound or a thermo-compressive bonding technique.

However, it is well known that Al on the rear side is not convenient for die bonding with most of available epoxy-based silver conductive pastes since the formation of Al_2O_3 on the surface poses a barrier and can cause deleterious instabilities during the functional period. Therefore additional metal layers should be superimposed to meet the requirements and overcome contact problems. Before depositing additional backside Ni and Au layers after the Al metal layers are once fabricated, *in situ* RF sputter etching is first utilized to remove the Al_2O_3 thin film from the backside Al layer. After the sputter deposition of the Ni and Au layer, the wafer dicing process took place and the additional thermal treatment tests and characterizations were further performed on individual devices.

To obtain an insight into the elemental depth distribution of the Au/Ni/Al multilayers, the interdiffusion processes, the formation of new phases and the presence of contaminants at the interfaces, the AES depth profiling was performed on an as-deposited sample and on a set of samples annealed at three different temperatures (623, 673 and 723 K).

The sample, which was not annealed, does not exhibit any mixing between the layers. The interfaces between individual layers are well defined and not contaminated as can be seen in Fig. 2 (dashed lines). Carbon and oxygen contamination at the surface can be ascribed to the sample manipulation prior to insertion into the analytical instrument.

The sample annealed at 623 K also revealed no appreciable interdiffusion. According to the depth profile of the as-deposited sample some insignificant redistribution occurred at the interfaces. Slightly broader transition regions on both sides of the Al layer can be attributed to the interface roughness, particularly caused by Al grains [3]. It can be also noted that Ni starts to diffuse into Al more intensely than vice versa already at this moderate temperature.

The AES depth profile of the sample annealed at 673 K (Fig. 2) differs significantly from the sample annealed at 623 K. Enhanced diffusion of Ni into the Al layer can be observed. Formation of a new phase is now clearly observed where the concentrations of Al and Ni tend to stabilize at a ratio of approximately 58% Al:42% Ni. The appearance of a new aluminide phase is in good agreement with the results of previous work [4].

Another process that is taking place is enhanced Ni diffusion in Au layer and its segregation at the Au surface. While at 623 K there is just an indication that Ni might be found at the surface, at 673 K this tendency is confirmed by detecting a higher content of Ni at the surface. Oxygen that is found as well at the surface forms the Ni oxide.

At 723 K the heat-assisted processes caused a new structural rearrangement, which reflects in a significantly different depth profile (Fig. 3). It is evident that Ni has diffused across the entire Al layer to the Al/Si interface and also that a reaction between Al and Ni has taken place. One of the possible reaction products between Al and Ni is NiAl [4]. A broader region of the new phase is observed and the concentrations of Al and Ni tend to stabilize at a ratio 55% Al:45% Ni.

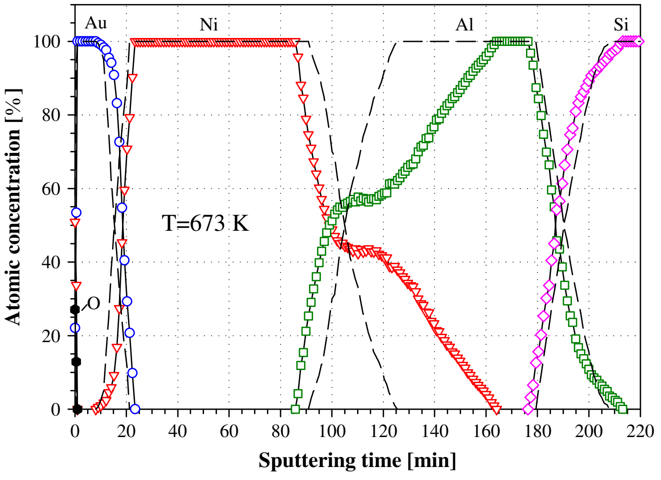

Fig. 2. AES depth profile of the Au/Ni/Al/multilayer on the Si substrate, annealed at 673 K. The depth profile of an as-deposited sample (dashed line) is shown for comparison.