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Thermal annealing, interface reaction, and lanthanum-based sub-nanometer EOT gate dielectrics

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ABSTRACT

In future nanoscale complementary metal-oxide-semiconductor (CMOS) devices, the high dielectric constant (high-k) gate dielectric film will be shrunk down to a couple of nanometers or down to the sub-nanometer range in the sense of oxide equivalent thickness (EOT). However, as high-k materials, including La_2O_3 which has been considered to be one of the promising next generation gate dielectric materials, are only marginally stable on the silicon substrate, some nominal temperature processes used for the device fabrication may still give rise to interface reactions and result in a low-k interface layer which will be a critical constraint for achieving the ultrathin EOT gate dielectric film. In this work, some issues related to the material interaction at the lanthanum oxide/Si and lanthanum oxide/metal interfaces will be discussed with the supports of interface bonding structures as revealed by using angle-resolved x-ray photoelectron spectroscopy (ARXPS) measurements. We show that thermal annealing at temperature above 500 °C would result in the migration of Si atoms deep into the bulk of the La_2O_3 film and formation of silicate phases both at the interface and in the bulk. These effects would significantly lower the dielectric constant and thus increases the effective thickness of the dielectric film from the equivalent silicon oxide thickness (EOT) point of view.

1. Scaling of CMOS gate length and equivalent oxide thickness (EOT)

The device feature size in the state-of-the-art CMOS technology, which has empowered the information technology revolution for decades, is being shrunk to a decananometer and that calls for a sub-nanometer EOT gate dielectric film [1–5]. In order to induce a sufficient amount of channel carriers with reasonable bias voltages, the gate capacitance should be scaled up accordingly by using either a thinner dielectric film or a higher dielectric constant (high-k) material. The gate dielectric thickness or EOT scaling is roughly in the same factor as the gate length reduction in earlier technology nodes. Aggressive gate dielectric scaling is even more favorable in several aspects [6]. However, the gate dielectric thickness scaling has been slowed down in the last decade partially due to relative conservative scaling scheme adopted for supply voltage, which made the device with thicker gate dielectric film still function well, but also the main reason was the difficulties encountered in producing subnanometer EOT gate dielectric films. For example, it was reported that EOT of over 1 nm or even SiO_2 was still used in 45 nm technology and in some advanced trigate structures [3,4]. The EOT reduction reported by Intel for 45 nm technology, based on Hf material, was 1 nm [3], and it reduced by 0.05 nm only for each generation. The EOT of Intel's 22 nm technology node was 0.9 nm [5,7]. Too much difficulty was encountered for further down scaling the hafnium-based, or other transition metal (TM) oxide gate high-k gate dielectrics from the technological point of view [8–10]. Fig. 1 illustrates the scaling trend of physical gate length and gate dielectric EOT as predicted by the International Technology Roadmap for Semiconductors (ITRS) in 2013 [11]. It can be seen that the gate length scaling is still quite optimistic. The physical gate length will be scaled from 20 nm to about 8 nm in a decade but the reduction rate in gate dielectric EOT is much slower. The EOT downsizing will be slowed down to about 0.03 nm for each technology node.

A feasible physical film thickness of high-k materials should be above 3 nm. With this connection, gate dielectric materials with

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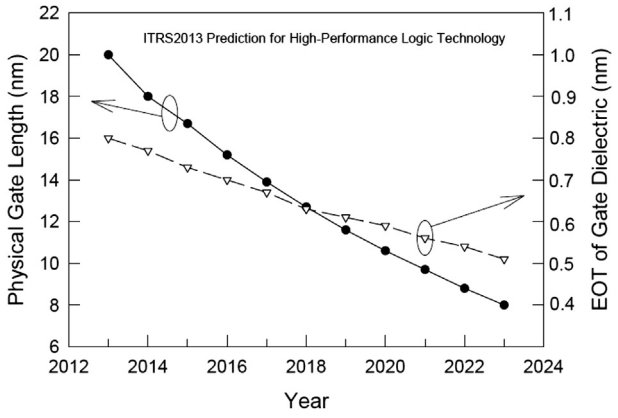

Fig. 1. Downsizing trends in gate length and gate dielectric EOT for high-performance logic technology as predicted by ITRS in 2013. EOT values were calculated based on data extracted from ITRS 2013 update [11].

higher dielectric constant will be indispensable. It was demonstrated that the rare earth (RE) lanthanum oxide or lanthana should be a promising candidate in the quest to satisfy this ultimate challenge [12–14]. Lanthana (La_2O_3), having a dielectric constant of 27 and a large conduction band offset of 2.3 eV with silicon, is well suited for this application. In principle, a 5-nm thick La_2O_3 should be equivalent to the conventional silicon dioxide of 0.7 nm thickness which is the physical limit of SiO_2 [2]. However, the actual EOT was found to be much larger mainly because of the transition low-k silicate layer between the La_2O_3/Si interface and the bulk dielectric constant of La_2O_3, depending on the preparation and processing conditions, was also found to be smaller than the expected k value [1,15–18]. In fact, the interfacial silicate layer becomes the lower boundary of the achievable EOT. For a high-k dielectric layer with a silicate interlayer (IL) of t_{IL} thickness, the minimum EOT will be given by:

$$EOT = t_{IL} + \frac{\varepsilon_{ox}}{k_{high-k}} t_{high-k} \quad (1)$$

where ε_{ox} and $k_{high\text{-}k}$ are the dielectric constants of silicon dioxide and the high-k material, respectively; $t_{high\text{-}k}$ is the physical thickness of the high-k film.

Thermal treatment of the stack can significantly increase the thickness of the low-k transition layer. The transition low-k layer has received much attention over the decades [19–21]. The interface layer was also found to have a strong influence on the device performance and reliability [1,20–24].

2. Instability and material interaction of lanthanum oxide

There are several fundamental problems associated with lanthanum and lanthanum oxide. Beside the higher k value, all the other aspects of high-k materials are poorer than the conventional silicon-based dielectric materials [1,2]. In particular, lanthanum oxide is an extrinsic material to the substrate silicon, it has a hygroscopic nature; it is marginally stable on silicon oxide and that causes the growth of a low-k interfacial layer at the normal processing temperature of the standard CMOS process [1,22]. The chemical reactions at the high-k/silicon interface cause most of the performance degradation issues. The conventional MOS layout for large scale integration is in a surface structure. The channel mobility of the transistors is predominately governed by the dielectric/silicon interface. Improvement of the SiO_2/Si interface property had been one of the major concerns since the invention of the MOS transistor even though the SiO_2/Si interface is almost perfect [26–29]; whereas the quality of high-k metal/Si interface was found to be much poorer. Transistors with higher channel mobility and other electrical performances were realized with a SiO_2 buffer layer inserted in between the high-k/silicon interface [3,20,21]. Lanthanum has low valance electron energy, larger oxygen chemical potential, and larger electronegativity [1]. These fundamental properties are much poorer than those of conventional silicon dioxide and may lead to several material interactions with silicon as well as silicon dioxide. Fig. 2 illustrates the possible reactions that may take place amongst these materials. These reactions are governed by the processing temperature. It was found that thermal annealing of high-k oxides has several impacts on the high-k/Si interfaces and makes the interface quality poorer than that of the SiO_2/Si interface. Fig. 3 illustrates the possible consequences at the high-k/Si interface and in the bulk of high-k materials when a thermal treatment takes place [1,2]. A low-temperature treatment, such as post-metallization or during deposition anneal, will help to release the interface strain created during previous processing steps. Higher temperature treatment will result in partial (in the nanometer scale) crystallization although the crystallization temperatures for bulk-type metal oxides are reported to be much higher. Different modifications of crystallized films would result in different band-gaps and effective masses [30] which may lead to quite different values of gate leakage current [22,23]. Thermal processing above 500 °C will result in interface oxidation and the formation of an interfacial silicate layer; both effects result in significant EOT enhancement. With the presence of a metal with a positive Gibbs-free-energy for oxygen change at high temperature, a reduction of the interfacial SiO_2 (so-called scavenging process) may also be possible [31,32]. This process leads to the EOT improvement. However, the La_2O_3/Si structure was found to have an EOT degradation at high temperature because of the formation of a low-k silicate layer although La has a quite large positive Gibbs-free-energy [31,32]. It was reported that a silicate layer of about 1 nm thick with dielectric constant in the range of 8–14 [18] was found in a 5 nm thick La_2O_3 film. That layer is too thick and the k value is too low for the present-day technology node. Since EOT is the primary concern of this work, we shall focus on the interface reactions that may be taking place during thermal treatment at temperatures in the range of 500–600 °C. At temperatures higher than 900 °C, serious crystallization, phase separation of silicate, or even, decomposition of the metal oxide will also be possible [1,29].

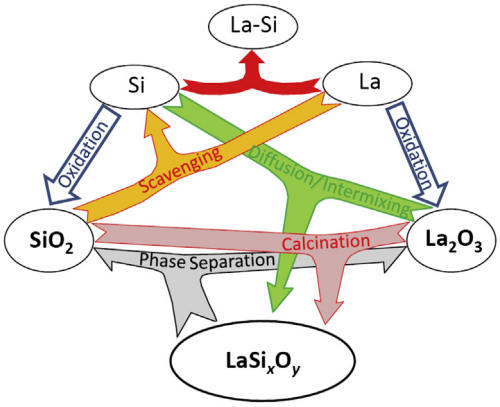

Fig. 2. Paradigm showing the possible chemical reactions amongst Si, La, SiO_2, La_2O_3, and $LaSi_xO_y$.