Vacuum 116 (2015) 96-103

Contents lists available at ScienceDirect

Vacuum

journal homepage: www.elsevier.com/locate/vacuum

Numerical simulation and experimental verification of vacuum directional solidification process for multicrystalline silicon

Guoqiang Lv ^{a, c}, Daotong Chen ^{a, c}, Xi Yang ^{a, b, c}, Wenhui Ma ^{a, b, c, *}, Tao Luo ^{a, b, c}, Kuixianai Wei ^{a, b, c}, Yang Zhou ^{a, b, c}

^a Faculty of Metallurgical and Energy Engineering, Kunming University of Science and Technology, Kunming 650093, China

^b State Key Laboratory of Complex Nonferrous Metal Resources Cleaning Utilization in Yunnan Province/The National Engineering Laboratory for Vacuum

Metallurgy, Kunming University of Science and Technology, Kunming 650093, China

^c Engineering Research Center for Silicon Metallurgy and Silicon Materials of Yunnan Provincial Universities, Kunming 650093, China

A R T I C L E I N F O

Article history: Received 12 January 2015 Received in revised form 6 March 2015 Accepted 11 March 2015 Available online 21 March 2015

Keywords: Numerical simulation Vacuum directional solidification Multicrystalline silicon

ABSTRACT

In this paper, a transient numerical model was applied to simulate the vacuum directional solidification (VDS) process of multicrystalline silicon (mc-Si) under different pulling-down rates, and the evolution of temperature distribution, thermal stresses and shape of solid/liquid (s/l) interface were simulated and analyzed. The experiments, such as the content and distribution of metal impurity, the crystal growth orientation and quality of mc-Si ingot were investigated to evaluate and validate the relationship between the thermal stresses and shape of s/l interface with simulation results. The results show that thermal stress, shape of interface s/l and temperature distribution in the silicon is determined by the thermal conditions in the furnace during the VDS process, and the crystal growth quality of mc-Si ingot relates closely to these factors. An appropriate pulling-down rate can satisfy thermal conditions to provide ideal temperature gradient in the silicon with lower thermal stresses and suitable s/l interface. We found that the mc-Si ingot produced by VDS process with pulling-down rate of 10 µm s⁻¹ had a larger grain size, a vertical columnar structure and an ideal efficiency of the impurity removal.

© 2015 Elsevier Ltd. All rights reserved.

1. Introduction

The metallurgical route is one of the most powerful and promising method in preparation of solar grade silicon (SoG-Si) directly from metallurgical grade silicon (MG-Si) because of its energy conservation and emission reduction [1]. The VDS technology is an effective method widely applied to remove metal impurities (such as Fe, Al, Ca, Ti, etc.) in silicon ingot casting via metallurgical method [2,3].

The distribution characteristics of metal impurities and the microstructures such as crystal type, grain size and defects of mc-Si ingot are determined by the temperature distribution and control of heat flow during the VDS process, so the heat transfer characteristics in which are worthy of in-depth study [4–7]. However, it's

difficult to measure and observe directly some important data in silicon material through experimental means during the VDS process, such as the temperature distribution, the shape and transformation of s/l interface, the flow pattern of silicon melt and the thermal stresses within silicon ingot. Numerical simulation makes an effective method for the study of the VDS for mc-Si. Over the years, many studies on analysis and optimization of solidification process of crystalline silicon for solar cells have been carried out [8–13]. Recently, numerical simulation is adopted for solving thermal stresses and the shape and transformation of s/l interface of the mc-Silicon during DS process. L.I. Liu et al. [14–16] performed numerical simulations and reported several improvement measures of DS furnace from the view of convection and mass transfer based on thermal field. They also obtained that thermal stresses can be reduced by a longer solidification time, and a crucible with large thermal expansion coefficient is recommended. C.E. Chang [17] confirmed that the shape of s/l interface can be adjusted by changing the temperature of the heaters. H. Miyazawa et al. [18] numerically investigated the influence factors on interface shape in DS Process and Y. Delannoy et al. [19] simulated the mc-Si





^{*} Corresponding author. Engineering Research Center for Silicon Metallurgy and Silicon Materials of Yunnan Provincial Universities, Kunming 650093, China. Tel.: +86 871 65161583; fax: +86 871 65107208.

E-mail addresses: lvguoqiang_ok@aliyun.com (G. Lv), mwhsilicon@163.com (W. Ma).

furnace using 3D dynamic mesh and had put forward some control methods of the interface, in order to improve the quality of crystal.

Although there have been some reports of study on thermal stresses or s/l interface shape relating to temperature field, the results of these reports are not of comprehensive considering of the influencing factors on crystal quality. In this paper, a transient numerical model was applied to simulate the VDS process for mc-Si under different pulling-down rates, and the evolution of temperature distribution, thermal stresses and shape of s/l interface were simulated and analyzed. Experiments were carried out, and the distribution and existence form of metal impurities as well as the growth orientation and quality of crystal were investigated to evaluate and validate the relationship between the thermal stresses and the s/l interface shape with simulation results.

2. Model description

Fig. 1 shows the configuration and computation grids of a VDS furnace for 2D global analysis with cylindrical crucibles. The system consists of quartz crucible, graphite susceptor, exchange block, graphite heaters, insulations, water cooled plate and furnace walls. The silicon feed materials are loaded into crucible with the diameter of 13 cm and height of 25 cm. During the VDS process, a suitable temperature gradient in the silicon material is maintained by adjusting the heating power and slowly moving components (crucible, susceptor, exchange block and water cooled plate) downwards with a constant pulling-down rate. Thermocouple 1 (TC1) is installed in the middle of upper and lower heater, while thermocouple 2 (TC2) is installed between the lower heater and the bottom of the side insulation. The automatic temperature controlling system will adjust heater power output to control the temperatures of TC1 and TC2 to match the pre-set values. The main

2 1 1: Melt 5 2: Crystal 3: Crucible 4: Susceptor 11 10 7-8: Heaters 9: Insulations 10: Pedestal 11: Furnace wall

Fig. 1. Model configuration for the cross-sectional area of the vertical furnace system.

assumptions in this model are as follows: (1) the convective movement of the free space airflow is ignored because the inside of furnace is in a vacuum condition, (2) the flow in silicon melt is mainly natural convection caused by the density changes which has less effect on the m/c interface, (3) all radiative surfaces are diffusegray. (4) the heat flux is led-out by the cooling water in the water cooled plate under the exchange block during the VDS process. The upper and the underside surface of the water cooled plate are set continuity boundary condition and constant temperature boundary condition, respectively.

Governing equations of the heat transfer in all components can be described as:

$$\rho C_p \frac{\partial T}{\partial t} = \nabla \cdot (k \nabla T) + Q \tag{1}$$

where ρ , C_p , and T are density, specific heat capacity, and temperature, respectively. The parameter k is thermal conductivity, and Q is the heat source term. The radiative heat exchanges between all gray and diffuse surfaces in the furnace were calculated by following equations:

$$-\overrightarrow{n}\cdot(-k\nabla T) = \varepsilon \Big(G - \sigma T^4\Big)$$
⁽²⁾

$$(1-\varepsilon)G = J - \varepsilon\sigma T^4 \tag{3}$$

where ε is the emissivity, G is irradiation, σ is called the blackbody radiation constant; *I* is radiosity. It is very important to accurately simulate the s/l interface for the transient simulation of VDS process. The s/l interface plot is theoretically the isotherm of 1685 K, which is the melting point T_m of silicon. With consideration of the calculation of the solidification latent heat, a dynamic interface tracking method was used. The release of latent heat was considered through the change in ΔH (enthalpy). In addition, the specific heat capacity C_p also changed considerably during the transition. To account for the latent heat related to the phase transition, we replaced C_p in the heat equation with $(C_p + \delta \Delta H)$, where ΔH is the latent heat of the transition and δ is a Gaussian curve given by

$$\delta = \frac{\exp\left[-\left(T - T_m\right)^2 / (\Delta T)^2\right]}{\Delta T \sqrt{\pi}}$$
(4)

where T_m is the melting point (1685 K) and ΔT denotes half of the transition temperature span which was set to 0.01 K in this case. The change in specific heat can be approximated as $\Delta C_p = \Delta H/T$, and represented by using software's built-in smoothed Heaviside step function. A fraction of liquid phase B is induced for dynamic meshing and interface tracking, given by

$$B = \begin{cases} 1, & T > T_m + \Delta T \\ (T - T_m + \Delta T)/(2\Delta T), & (T_m - \Delta T) \le T \le (T_m + \Delta T) \\ 0, & T < T_m - \Delta T \end{cases}$$
(5)

The distribution of *B* reflects directly the position and shape of the solid/liquid interface (Actually, either to plot with the isotherm of T_m or from the distribution of *B*, we get the same interface shapes since the temperature span ΔT is rather small).

The stress-strain relation for thermo-elastic solid body can be given by the following formulation:



Download English Version:

https://daneshyari.com/en/article/1690422

Download Persian Version:

https://daneshyari.com/article/1690422

Daneshyari.com