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Study of inductively coupled Cl_2/BCl_3 plasma process for high etch rate selective etching of via-holes in GaAs

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ABSTRACT

We have investigated the selective etching of 50 μm diameter via-holes for etch depth >200 μm using 30 μm thick photo resist mask in Inductively Coupled Plasma system with Cl_2/BCl_3 chemistry. Resultant etch rate/etch profiles are studied as a function of ICP process parameters and photo resist mask sidewall profile. Etch yield and aspect ratio variation with process pressure and substrate bias is also investigated at constant ICP power. The etch yield of ICP process increased with pressure due to reactant limited etch mechanism and reached a maximum of ~19 for 200 μm depth at 50 mTorr pressure, 950 W coil power, 80 W substrate bias with an etch rate ~4.9 μm/min. Final aspect ratio of etched holes is increased with pressure from 1.02 at 20 mTorr to 1.38 at 40 mTorr respectively for fixed etch time and then decreased to 1.24 at 50 mTorr pressure. The resultant final etch profile and undercut is found to have a strong dependence on the initial slope of photo resist mask sidewall angle and its selectivity in the pressure range of 20–50mTorr.

1. Introduction

GaAs devices are used extensively in the wireless telecommunications industry, where the high electron mobility of GaAs makes it well suited for high frequency, low noise and high gain applications. Although it has excellent electrical properties, GaAs is a relatively poor thermal conductor, making it difficult to remove heat efficiently from power devices. A commonly used solution is to form via-holes grounds from the wafer backside to the front side circuitry. Such connections provide a good thermal path for heat removal as well as a low impedance ground for RF (radio frequency) devices. This backside via formation is one of the final steps in the device fabrication. After completion of the front side processing, the wafer is mounted face down on a carrier wafer and mechanically thinned to a thickness of approximately 100–200 μm. The back of the wafer is then patterned using photo resist and the holes are etched using reactive ion etching (RIE) through the thinned substrate, stopping on the front side metal. After resist removal the vias are metallized, typically by sputtering a gold seed layer followed by gold electroplating to act as the heat sink/ground connection [1].

Inductively Coupled Plasma (ICP) etching has been replacing conventional RIE for GaAs backside via etching because of several advantages. Throughput improvement utilizing significantly faster etching rate have already been reported in the literature [2]. Furthermore, the ICP tools provide better control of via size, repeatability and reproducibility [3,4]. The ICP tools produce significantly different via dimension as compared to the conventional RIE tools, if the same size mask used, due to its nature of etching process. The etch profile and surface morphology of via-hole grounds is important not only for the inductance consideration but also for the success of backside metallization. The smooth morphology of the etched sidewalls provides reliable and good electrical contact with low resistance. Etching is mainly carried out in chlorine/fluorine plasma. A number of gas combinations CCl_2F_2, CCl_2F_2/CCl_4, $SiCl_4/Cl_2$, $BCl_3/Cl_2/Ar$, Cl_2/Ar and Cl_2/BCl_3 have been utilized to fabricate via-holes [4]. Each gas combination has its advantages and disadvantages. The previous work reported using $Cl_2/BCl_3/Ar$ for etching of GaAs is mainly carried out using RIE for etch depths ~100 μm and etch rate reported are much lower ≤1 μm/min for 3-inch GaAs wafer. Cl_2/BCl_3 gas mixture with ICP process is being increasingly used for fabrication of via-holes at high etch rates with excellent anisotropy and smooth surface morphology. Generally reported etch depths using ICP for via-hole etching applications in GaAs Monolithic Microwave Integrated Circuits (MMIC) are less than 200 μm using photo resist mask due to lower etch rate and poor mask selectivity. The substrate

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thickness of ≥200 μm is preferable as it results in higher yield and throughput due to easier handling of fragile wafers without carriers and also improves the RF performance due to lower electrical losses in MMIC micro strip interconnects on the front side.

It is not easy to etch 200 μm deep holes at high etch rates with desired profile, good reproducibility and repeatability as etching depends upon various parameters like component of radicals, ions in plasmas, flow of gases, dc bias and type of mask used. Therefore, it becomes important to understand the effect of these plasma parameters on etch rate, anisotropy, etch profile, aspect ratio, mask selectivity and then develop the process for particular application [3–6]. The etch rate is the GaAs thickness etched in 1 min (μm/min.), anisotropy is defined as {1 − (lateral etch rate/vertical etch rate)}, etch profile refers to the shape of etched feature cross-section, aspect ratio is etch depth/feature's lateral dimension and selectivity is defined as the etch rate of GaAs/etch rate of photo resist mask.

We are reporting the ICP etching process of 50 μm diameter via-holes at relatively high average etch rate for an etch depths of ~200 μm, on 3-inch GaAs wafer using positive photo resist mask. As etch depth increases, etch rate reduces drastically, with photo resist mask, affecting process throughput significantly in a production environment. Etch rate variation with ICP process parameters i.e. pressure and substrate bias power, are studied in detail at a constant maximum available ICP coil power to have high plasma density that results in high etch rates. At high plasma density, pressure and bias voltage are the most important parameters to control etch profile and selectivity as they mainly control the ion energy i.e. physical component of etching. Aspect ratio and etch yield are two important parameters that characterise any etch process [7–9]. Variation of aspect ratio and etch yield with process parameters is also studied. As thick photo resist mask is required to etch deep holes, its sidewall profile and selectivity plays an important role in deciding the final etch profile. We are also reporting this effect by varying sidewall angle of photo resist mask [10].

To our knowledge these parameters for an ICP etch process involving etch depths of ~200 μm with such high average etch rates have not been reported so far using Cl_2/BCl_3 chemistry. The main purpose of the study was to develop a relatively high etch rate, production viable ICP etching process to etch ~200 μm deep via-holes with acceptable via-hole etch profile, photo resist mask selectivity and etch uniformity for fabricating 50 μm diameter via-hole ground connections in GaAs MMICs over a 3-inch wafer.

2. Experimental details

All test wafers were 3-inch S.I. GaAs wafers with thickness ~650 μm these wafers were then coated with in 30 μm thick positive photo resist AZ 4620 and patterned with 50 μm diameter holes. The patterned photo resist was then post baked at 120 °C for variable time to introduce a sloped photo resist profile with improved adhesion. These patterned wafers were then mounted on a carrier wafer with wax to make wafer loading compatible with ICP system and also provide cooling of the wafer during etching process.

The patterned wafers were then etched in standard ICP system, one at a time. Plasma of etcher is inductively coupled through a coil at 13.56 MHz, with independent energy control provided by 13.56 MHz RF biasing on the substrate. Helium gas was used to cool backside of the wafer. The substrate temperature was set at 20 °C for all test conditions. The etch chemistry was a mixture of Cl_2/BCl_3 through mass flow controlled process gas lines. The chamber was evacuated to a base pressure of 9e-3 mTorr, by a turbo molecular pump backed by a dry mechanical pump, before initiating the etch process. The etch gases mixture was introduced through an annular region at the top of chamber lid. ICP etching was carried out using only photo resist mask to have less complex process with good etch surface morphology. All the ICP experiments were carried out at near-maximum available coil power and Cl_2/BCl_3 flow rate ratio of 4:3 for a fixed total flow rate ~280 sccm to have high plasma density [11] and increased concentration of reactive Cl species, that

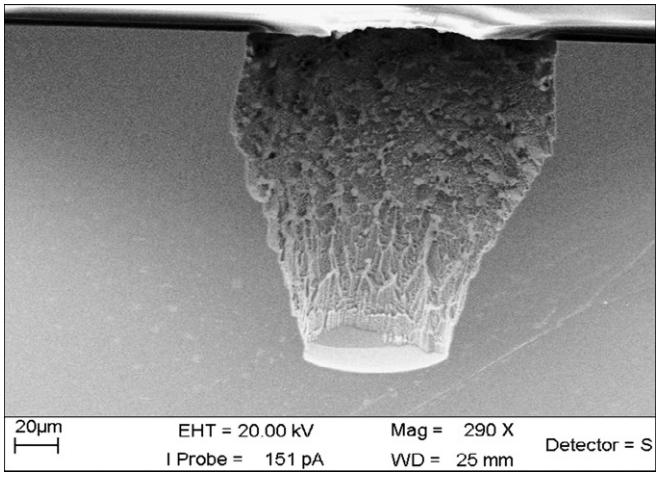

Fig. 2. SEM cross-section of hole etched upto a depth of more than 175 μm.

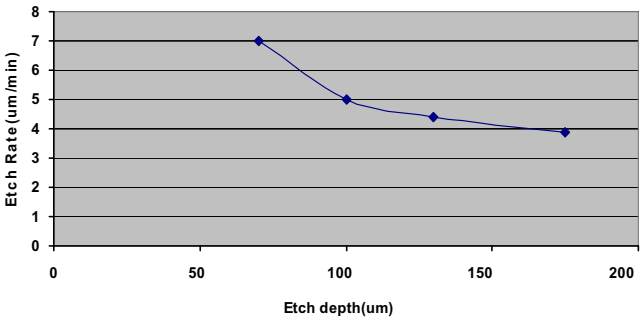

Fig. 1. Etch rate as function of etch depth (950 W ICP Power, 65 W Substrate bias and 30 mTorr).

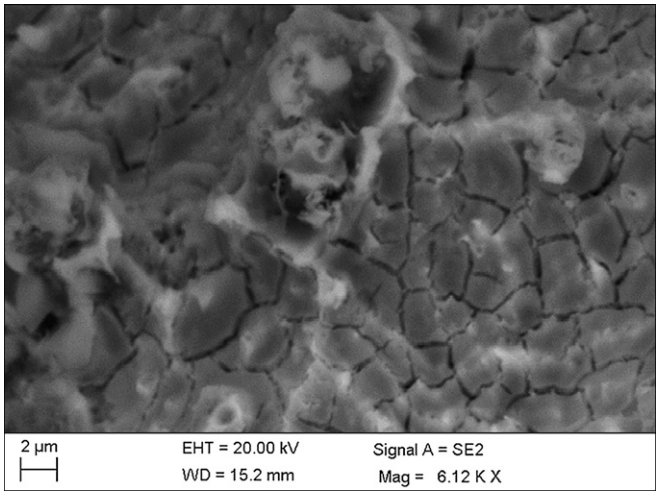

Fig. 3. SEM photograph showing deposition on the etched sidewall.