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Improvement of electro-physical properties of ultra-thin PECVD silicon oxynitride layers by high-temperature annealing

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Abstract

Ultra-thin (5 and 6 nm) silicon oxynitride layers have been fabricated by the plasma-enhanced chemical vapour deposition (PECVD) process. Split experiments with annealing of the deposited dielectric layers were performed using the RTP reactor and a standard furnace, both at 900 °C. Possible changes in properties, structure and chemical composition of the obtained layers were investigated by means of spectroscopic ellipsometry, X-ray photoelectron spectroscopy (XPS), secondary ion mass spectrometry (SIMS) and electrical characterisation of manufactured test structures (metal–insulator–semiconductor (MIS) capacitors and MISFETs). The results achieved have shown that annealing at high temperature causes improvement of the properties of ultra-thin silicon oxynitride layers (e.g. lower interface traps density, lower leakage currents within the dielectric layer and lower charge-pumping currents of the MISFETs). The observed improvement in electro-physical properties can be attributed to the increase of the SiON phase. Moreover, comparison between the physical thickness and the equivalent oxide thickness (EOT) of the layers shows a decrease in physical thickness obtained by using the silicon oxynitride layer instead of the classical silicon dioxide. These findings are important for the consideration of chances of PECVD oxynitride layer application for CMOS technology.

Keywords: Ultra-thin dielectrics; Silicon oxynitride; PECVD; CMOS; SIMS; XPS

1. Introduction

Extremely high demands of the ITRS Roadmap forced a drastic reduction of the gate dielectric layer's thickness applied in advanced CMOS ICs [1]. However, in the past years a range of fundamental limitations have appeared. The electro-physical properties of the most known and well-investigated insulator commonly used as the gate dielectric layer—silicon dioxide (SiO_2)—have demonstrated to be insufficient, while the thickness has been decreased to its technological limit [2]. Thus, to maintain the same capacitance without increasing the gate transistor dimensions, dielectric layers with permittivity constant higher than that of SiO_2 have to be used.

Silicon oxynitride (SiO_xN_y) seems to be a promising substitute for SiO_2 as the gate dielectric in CMOS–ULSI technologies [3]. This is mainly due to the fact that the dielectric constant of oxynitride is slightly higher than that of SiO_2, the reliability of the oxynitride/silicon system is higher and boron and phosphorus diffusion is reduced. Moreover, the diffusion of atomic hydrogen is also reduced by SiO_xN_y when compared with standard SiO_2 [4].

However, during standard CMOS, self-aligned technology electrical activation of the implanted dopants by high-temperature annealing occurs after the gate dielectric fabrication [5]. This process, performed by annealing either in the furnace or in RTA reactor, may obviously influence stability and electro-physical properties of gate dielectric layers [6,7]. Hence, in order to establish suitability of the

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ultra-thin dielectric layers for CMOS technology, it is important to be aware of the properties of these layers "after annealing" and not only "as deposited".

This paper examines the effects of such high-temperature annealing of ultra-thin PECVD SiO_xN_y layers. Changes in structure, chemical composition and electro-physical properties were described and examined by means of X-ray photoelectron spectroscopy (XPS), secondary ion mass spectrometry (SIMS) and electrical characterisation.

2. Experimental

The ultra-thin SiO_xN_y layers were deposited in an Oxford PlasmaLab System 80+. Two sets of the SiO_xN_y layers with different thicknesses were chosen to perform investigations—5 and 6 nm. Non-self-aligned NMOS technology was used to fabricate test structures (MOS capacitors and MISFETs) onto 2-in silicon ⟨1 0 0⟩ 'p' type substrates (4–7 Ω cm resistivity) cleaned just prior to processing by the RCA method. Split experiments with annealing of the deposited dielectric layers were performed using the RTP reactor and standard furnace, both at 900 °C. In order to mimic the dopant activation annealing in CMOS technology, the time duration of these processes were 10 s and 30 min, respectively. The annealing processes in the RTP proceed in different atmospheres: argon, nitrogen and hydrogen diluted in nitrogen (1:5 ratio). In the furnace, only argon gas was applied for the annealing. In this paper, the following names are used to refer to the types of processes studied: 'as deposited'—for the oxynitride layers without any annealing steps, 'RTP Ar', 'RTP N', 'RTP N + H'—for the layers annealed in RTP reactor in respective gases and 'furnace'—for the layer annealed at high temperature in argon in the furnace.

A J.A.Woollam Co. ellipsometer allowing measurements at different angles of incidence with the wavelength ranging from 250 to 1100 nm was used to determine the thickness and refractive index of the investigated layers.

The XPS measurements were performed with the Mg Kα excitation at 1254 eV at the Brandenburg University of Technology in Cottbus. The samples were cleaned in an acetone ultrasonic bath before being introduced into the ultra-high vacuum (1.33×10^{-7} Pa).

The SIMS measurements have been conducted using the SAJW-05 instrument with the quadrupole-based mass analyzer Balzers (QMA-410). The apparatus is also equipped with 06-350E Physical Electronics Ar^+ ion gun. The samples were sputtered with Ar^+ primary ions at 880 eV impact energy. The use of ultra-low energy primary beam for sputtering helped us to reduce atomic mixing and, in consequence, to get profiles with high depth resolution. The ion beam of about 100 μm in diameter at 70 nA current was rastered over a 2000 μm × 3000 μm area. Quantitative atomic concentration of nitrogen and oxygen was calculated based on Si_2N^+, Si_2O^+ and Si_2^+ secondary ion currents following the calibration procedure described in [8].

The electrical measurements were performed with the Hewlett-Packard 4061A Semiconductor Component Test System (*C–V* characteristics) and Keithley SMUs (*I–V* characteristics). The metal–insulator–semiconductor (MIS) capacitors with a gate area of $A = 1.7 \times 10^{-5}$ (for *C–V* characteristics measurements) and 4×10^{-4} cm^2 (for *I–V* characteristics measurements) were used allowing the determination of basic electro-physical properties of the investigated layers. Moreover, charge-pumping currents of test MISFETs ($W \times L = 10\,\mu m \times 10\,\mu m$) were measured to evaluate the interface trap density (D_{it}) according to [9]:

$$I_{cp_{max}} = A_G q f D_{it},$$

where $I_{cp_{max}}$ is the maximum CP current obtained from the charge pumping measurements, A_G is the gate area, q is the elementary charge, f is the gate signal frequency and D_{it} is the total surface density of interface traps.

3. Results and discussion

Study of the ultra-thin PECVD SiO_xN_y layers structure and composition were performed by means of XPS measurements analysis. To obtain information about the chemical bonds present in the dielectric layer, the measured spectra were analysed by deconvolution of the spectrum lines. Every single line was attributed to the particular compound, due to its unique binding energy in the ultra-thin dielectric layer. A survey spectrum of the 'as deposited' oxynitride is shown in Fig. 1. Strong O1s (~530 eV), N1s (~400 eV) and Si2p (~100 eV) peaks can be seen. The C1s (~290 eV) peak is also visible, but this carbon must have originated from ex-situ XPS measurements.

Fig. 2 shows comparison of compositions of layers, both 'as deposited' and annealed in RTP reactor, expressed in terms of the effective thickness (using ellipsometric thickness of each layer). The thicknesses of the dielectric layers were evaluated from the measurements assuming the 'Cauchy' model [10].

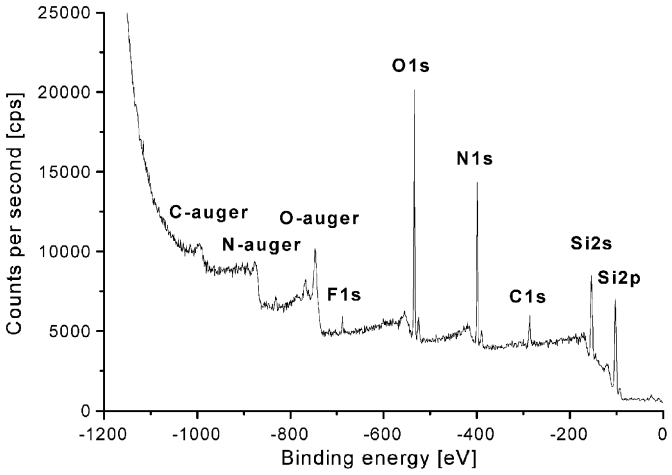

Fig. 1. Survey spectrum of 'as deposited' PECVD silicon oxynitride layer.