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Digital and analog integer delayed modeling and control for multivariable systems with multiple time delays in states, inputs and outputs

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ABSTRACT

This paper presents a new approximated integer delayed modeling and control technique for Continuous-time Fractional Delay Differential Equations (CFDDEs). Using the impulse response sequences of the CFDDE and the balanced model-reduction method, a delay-free discrete-time state-space model is constructed. Then, an equivalent Discrete-time Integer Delay Difference Equation (DIDDE) is obtained by transforming the obtained discrete-time state-space model into a controller-type block companion form. Furthermore, based on the obtained DIDDE, an equivalent Continuous-time Integer Delay Differential Equation (CIDDE) is determined by means of the newly developed Chebyshev's bilinear approximation method. For digital control of the CFDDE, an optimal Discrete-time Integer Delayed Control Law (DIDCL) is designed using the conventional discrete-time LQR approach together with the obtained delay-free discrete-time state-space model. On the other hand, for continuous-time control of the CFDDE, a Continuous-time Integer Delayed Control Law (CIDCL) is determined from the designed DIDCL by means of the inverse Chebyshev's bilinear approximation method. Finally, digital and analog integer delayed observers are constructed for the implementations of the developed DIDCL and CIDCL, respectively. An illustrative example is given to demonstrate the effectiveness of the proposed method.

1. Introduction

Industrial processes are often represented by a linear difference-differential state-space model with multiple (fractional/integer) time delays in the state, input and output as,

$$\dot{x}(t) = \sum_{j=0}^{N_x} A_j x(t - T_{x_j}) + \sum_{j=0}^{N_u} B_j u(t - T_{u_j}),$$
$$y(t) = \sum_{j=0}^{N_y} C_j x(t - T_{y_j}), \tag{1}$$

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where $A_j \in \mathbf{R}^{n\times n}$, $x(t) \in \mathbf{R}^{n\times 1}$, $B_j \in \mathbf{R}^{n\times m}$, $u(t) \in \mathbf{R}^{m\times 1}$, $C_j \in \mathbf{R}^{p\times n}$ and $y(t) \in \mathbf{R}^{p\times 1}$. The different fractional/integer delay times $T_{x_j} \geq 0$, $T_{u_j} \geq 0$ and $T_{y_j} \geq 0$ are the delays corresponding to the jth state, input and output, respectively. In addition, the integer index numbers $N_x \geq 0$, $N_u \geq 0$ and $N_y \geq 0$ represent different multiple time delays for the state, input and output, respectively. The stability, controllability and observability of the multiple time-delay system given by (1), which is called Continuous-time Fractional Delay Differential Equation (CFDDE), have been analyzed in the literature [1–6]. The memory-less (delay-free) continuous-time controllers for the continuous-time multiple time-delay systems in (1) have been developed in [1,7–10]. Furthermore, for discretization of a continuous-time system with both state and input delays, an exact discretized quasi-autoregressive moving average (QARMA) model has been proposed and approximately implemented via a finite impulse response filter in [11]. Meanwhile, for stabilization of a continuous-time system with state delays, a dynamic output-feedback controller has been developed in [12]. In addition, to achieve an optimal analog performance, a sampled-data model with a long state delay and a digital fractional filter design technique, based on the sampled-data H^∞ optimization method, have been developed in [13]. However, the development of the point-wise delayed (integer delayed) controllers [14] for the digital/analog control of the CFDDE in (1) has not been fully explored [1,4], but only partially developed (i) for continuous-time integer delayed control of the CIDDE in recent pioneer works [4,5,15,16], and (ii) for discrete-time delay-free control of the CFDDE in [17–19]. It is well-known that the design of a discrete-time controller for digital control of a continuous-time fractional state-delay system is a difficult task. This is due to the fact that it is difficult to determine a discrete-time state-space model which is an exact equivalent of a continuous-time system with multiple fractional time delays in the states. This is true even if the system's input functions are piecewise-constant, because the inter-sampled states evaluated at the fractional sampling times are not piecewise-constant. Hence, an approximated discrete-time state-space model [17,19] is often constructed. In this paper, we propose a new approximated digital and analog integer delayed modeling and control technique for the CFDDE in (1).

The objectives of this paper are described as follows:

Objective 1: Determine the Discrete-time Integer Delay Difference Equation (DIDDE) from the CFDDE in (1) as,

$$\begin{aligned} x_d(kT+T) &= \sum_{j=0}^{N_{x_d}} \hat{G}_j x_d(kT-jT) + \sum_{j=0}^{N_{u_d}} \hat{H}_j u_d(kT-jT), \\ y_d(kT) &= \sum_{j=0}^{N_{y_d}} \hat{C}_j x_d(kT-jT), \end{aligned} \tag{2}$$

so that,

$$x_d(kT) \text{ in (2)} \cong x(t)|_{t=kT} \text{ in (1)}, \tag{3a}$$

$$y_d(kT) \text{ in (2)} \cong y(t)|_{t=kT} \text{ in (1)}, \tag{3b}$$

are satisfied, considering that,

$$u_d(kT) \text{ in (2)} = u(t) = u(kT) \text{ for } kT \leq t < (k+1)T \text{ in (1)}. \tag{3c}$$

Objective 2: Determine the Continuous-time Integer Delay Differential Equation (CIDDE) from the CFDDE in (1) as,

$$\begin{aligned} \dot{x}_c(t) &= \sum_{j=0}^{N_{x_c}} \hat{A}_j x_c(t-jT) + \sum_{j=0}^{N_{u_c}} \hat{B}_j u_c(t-jT), \\ y_c(t) &= \sum_{j=0}^{N_{y_c}} \hat{C}_j x_c(t-jT), \end{aligned} \tag{4}$$

so that,

$$x_c(t) \text{ in (4)} \cong x(t) \text{ in (1)}, \tag{5a}$$

$$y_c(t) \text{ in (4)} \cong y(t) \text{ in (1)}, \tag{5b}$$

are satisfied, considering that,

$$u_c(t) \text{ in (4)} = u(t) \text{ in (1)}. \tag{5c}$$

Objective 3: Find the Discrete-time Integer Delayed Control Law (DIDCL) as,

$$u_d(kT) = -\sum_{j=0}^{N_{x_d}} K_{d_j} x_d(kT-jT), \tag{6}$$

so that digitally controlled sampled-data system of (6) and (1) achieves the desirable design goals.