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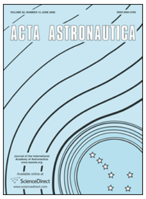

1-Bit processing based model predictive control for fractionated satellite missions

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ABSTRACT

The model predictive control (MPC) has great advantages in dealing with complex control constraints. However, traditional MPCs are too complex to implement in real-time embedded systems. This is especially true for nano-satellites due to limited on-board resources. This paper introduces a novel 1-bit processing based MPC (OBMPC) algorithm for a fractionated satellite mission, which can significantly reduce online calculations by removing multiply operations. The resulted pulse signals can be used to drive the actuator directly. The quantized state feedback fits the OBMPC in the frame work of quantized MPC. The stability issues and the design criterion are discussed in this paper. The simulation is based on a 2U CubeSat model in a fractionated satellite structure, in which the payload and actuators are separated from the controller and controlled via wireless inter-satellite link (ISL). Compared to the equivalent traditional MPC controller, FPGA implementation based performance analysis shows that OBMPC is feasible for fractionated satellite missions.

1. Introduction

The purpose of this paper is to propose a 1-bit processing based model predictive control (OBMPC) algorithm for satellite attitude control in a fractionated satellite mission. The concept of fractionated satellite is becoming popular for its flexibility and survivability compared to the traditional mono-satellite. In such system, satellite subsystems are not central in location but “fractionated” and “distributed” as “slave” satellites in the space, forming physically independent modules, and controlled by master satellites [1]. Such fractionated components not necessarily maintain the integrity as autonomous satellites but only play as one of the subsystems through wireless communication in the concept of monolithic spacecraft. However, such a structure normally has less onboard resources in terms of power and area for each fractionated subsystem. It is also a challenge to maintain the networked control system (NCS) for individual fractionated satellites via inter-satellite link (ISL) due to data loss and time delay (see [2] for a survey for NCS). In this work, we took the advantage of bi-level $\Delta\sum$ modulators for both control and communication, and developed an OBMPC algorithm for the proposed fractionated satellite mission.

Model Predictive Control (MPC) is highly attractive for spacecraft attitude control as it can deal with constrained non-linear control systems. However, the main problem for a MPC controller is that it requires on-line optimization, which is computation-intensive for embedded systems. This is especially true for nano-satellite missions due to limited onboard resources. Considerable research has been done to decrease the computational demand for MPC. As direct implementation of the MPC algorithm on the high-fidelity model is not feasible in time-critical systems, various model reduction methods (e.g. [3–5]) have been developed to decrease the system order while maintain the same properties of the model, such as the stability and passivity. However, the online calculation is

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still intensive, especially for real-time control systems with a high sample rate. Another notable approach is made by developing the Explicit MPC algorithm e.g. [6–8], which maps the state to the optimal input as a piecewise affine function, so that finding the optimal control law is restricted to a lookup-table, depending on the current state vector [6]. The EMPC is further developed for spacecraft attitude control [9] as one of the few practical studies for spacecraft attitude control using MPC. Furthermore, if one consider the limited processing resources as constraints to the control system, some efforts have been developed such as block model predictive control (a hybrid control scheme, which uses two different sampling intervals when the processing resources limitation changes [60]); choosing sub-optimal solutions for the MPC controller when computing resources are scarce [61,62]. Such trade-off between successive iterations in the MPC algorithm and the computational delay mirrors *anytime algorithms* using model reduction [63] or switching among a set of pre-designed controllers [64] and *sequence-based anytime algorithms* [65] which utilize extra processor availability to calculate control sequences as potential sub-optimal solutions.

The OBMPC algorithm uses bi-level Delta-Sigma ($\Delta\sum$) Modulators in the control loop. Such design can fit into the frame work of quantized receding horizon control, e.g. [10–13]. The system is in digital control nature, affected by quantization noise introduced by $\Delta\sum$ Modulators. The stability issue for such control system attracted a vast amount of literature e.g. [14–17]. The proposed OBMPC encodes sensing and control signals into a binary format, and process such binary signals directly without demodulation (namely 1-bit processing, [24]) to obtain optimal solutions. A high sampling rate (Over Sampling Ratio, OSR) is necessarily required to achieve high resolution of 1-bit processing. Delta operator is adopted in predictive control [18–23] to deal with the numerical issues introduced by the OSR. With 1-bit processing, all the multiplications can be simplified by changing the signs of the multi-bit coefficients. This makes MPC algorithms feasible for real-time control applications with high sampling frequencies. Many other benefits for the 1-bit processing include: (1) It retains the advantages of digital-processing techniques while approaching high quality analogue processors [24]; (2) The control performance is not affected by data loss due to the modulation techniques [25]; (3) Only 1-bit A/D converters are needed in the control loop, and D/A converters or pulse width modulation (PWM) logics are not necessary as 1-bit signals can nearly drive physical systems directly. For the sensing part, it is worth noting that considerable effort is being invested to embed the sensing device in a $\Delta\sum$ Modulator control loop, e.g. MEMS gyroscopes (see [26] for a recent survey). This allows the controller to acquire 1-bit signal directly from sensing components. In the simulation, the structural data and satellite model are based on a 2U CubeSat, which is developed for the international QB50 project [27] by the University of Sydney.

The remaining paper is organized as follows. In Section 2, 1-bit processing with $\Delta\sum$ Modulation is introduced. In Section 3, a novel 1-bit processing based MPC (OBMPC) algorithm is discussed. The stability issue is also developed in this section. In Section 4, a nano-satellite used in a fractionated satellite structure is modeled to validate the proposed OBMPC control algorithm. Section 5 compares the simulation results between the OBMPC and the traditional MPC in Matlab. The efficiency of the OBMPC is also compared in terms of power and area with the traditional MPC by FPGA implementations. Section 6 concludes.

2. Delta-sigma modulation and 1-bit processing

2.1. Delta-sigma modulation and 1-bit processing

The concept of 1-bit processing is based on the bi-level $\Delta\sum$ modulator (a throughout study of $\Delta\sum$ modulation and its stability issues can be found in [14]. Bi-level $\Delta\sum$ modulator is one of the most commonly adopted structures due to its circuit simplicity). Such a modulator featuring a bi-level quantizer, produces a single-bit pulse signal output which can be processed directly by controllers or drive dynamic models directly. This signal type is also known as pulse density modulation (PDM), which can be used in the satellite attitude control system to deal with the on–off nature of the satellite actuators [29], e.g. thrusters. Fig. 1 illustrates a general model of a high order $\Delta\sum$ modulator,
where a bi-level quantizer q_Δ is defined as

$$q_\Delta(x) \triangleq \begin{cases} \Delta & \text{if } x \ge 0 \\ -\Delta & \text{if } x < 0 \end{cases} \tag{1}$$

A bi-level $\Delta\sum$ modulator is popular due to the circuit simplicity and the binary nature of the quantizer output. However, to approach high resolution performance, OSR is required for $\Delta\sum$ modulation. If the frequency of interest is from 0 to f_0, the OSR is defined to be the ratio of the sampling frequency f_s to the Nyquist frequency $2f_0$:

$$OSR \triangleq \frac{f_s}{2f_0} \tag{2}$$

For decoding, decimation is required. The corresponding multi-bit digital format Y_q of the input U_q is determined by the following equation:

$$Y_q = \frac{1}{OSR}\sum_{i=1}^{OSR} q_\Delta(\hat{U}_q)_i, \tag{3}$$

where $\hat{U}_q$ is integrator's output with respect of the input U_q, and $q_\Delta(\hat{U}_q)$ is the output of the quantizer q_Δ. If $\hat{U}_q$ is positive or 0, $q_\Delta(\hat{U}_q)$ is $+\Delta$. If $\hat{U}_q$ is negative, then $q_\Delta(\hat{U}_q)$ is $-\Delta$. The output after decoding is limited to $-\Delta$ and $+\Delta$. In fact, 1-bit signals contain all the useful information of the input, but this information is obscured by the errors, in other words, the quantization noise [24].

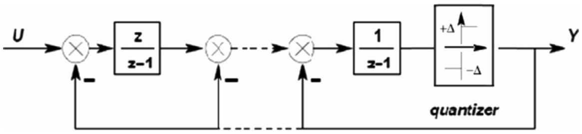

Fig. 1. High order $\Delta\sum$ modulator.