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Half bridge topology 500 V pulser for ultrasonic transducer excitation

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ABSTRACT

Application of half bridge topology for ultrasonic transducer excitation using long pulse trains is presented. The novelty of the approach is the high speed solution for a high side drive. A commercially available high speed digital isolator and a high speed MOSFET driver were combined to give the possibility to deliver fast driving signals to a high side N-channel MOSFET. The experimental investigation indicates that the output amplitude of the fundamental harmonic can reach 624 Vp–p for light loads and 552 Vp–p when driving 50 Ω loads. The operation frequency at such voltages can reach 10 MHz for unloaded or 50 Ω load condition and 6 MHz when driving capacitive 3000 pF loads. The output impedance is 13 Ω for voltages below 500 Vp–p and 16–26 Ω for voltages 500 Vp–p and above.

1. Introduction

The design of the high voltage pulser for ultrasonic transducer excitation is a challenging task when high voltage and relatively high frequency range is considered. Piezoelectric transducer is the most common type thanks to its simplicity, sensitivity and price. It exhibits capacitive load. Transducer excitation in ultrasonic imaging is usually performed using high voltage spike or single rectangular pulse [1,2]. The inspection of the composite materials requires high energy signals with frequencies up to 5 MHz [3]. Low frequencies can go down to 1 kHz when testing concrete [4]. Sonoporation [5] involves the usage of ultrasound to deliver therapeutic/genetic compounds into target cells. Such experiments would need long tonebursts. Up to 500 Vp–p output is required in order to reach high acoustic pressures [5]. The frequency used is based on contrast agent resonant frequency and covers a wide range: from 20 kHz up to 5 MHz frequencies [5]. Arbitrary pulse trains are needed in order to study swept frequency and random frequency effects. Then there is a need for 1 kHz to 5 MHz pulser capable to produce rectangular pulse trains or tonebursts up to 500 V into piezoelectric transducer or 50 Ω load.

Plenty of publications exists that are offering topologies for high voltage pulse generation [1,2,6–8]. Unfortunately, these topologies are intended for single pulse production and are not capable of long low frequency pulse trains generation or are not efficient. Capacitance of the transducers can reach 3000 pF which will alter the bandwidth of the pulser. This effect will be severe for the pulsers intended for a single pulse excitation, where only one front is steep. Capacitive load also reduces the efficiency of excitation since the energy that is not consumed by transducer is fed back to the pulser. This is not the issue when short excitation pulses are used since energy per pulse is low. But average power dissipated in pulser circuit can become large when long tonebursts or spread spectrum pulse trains are employed. For this reason, commercial pulsers are usually specified for resistive load, are bulky and expensive [9–11]. Capacitance reduction can be achieved by matching circuits [12] but high impedance of the circuit could remain. Typically, the transducer capacitance does not exceed 500 pF. When driving such light loads intrinsic losses of the pulser dominate. If the energy dissipated in the pulser circuit is minimised, then the size of the pulser can be reduced.

Such pulser is reported in [13]. It can operate down to low frequencies, produce up to 1 kV pulses and is able to produce long tonebursts. Nevertheless, its operation frequencies are limited to 1 MHz due to high side driver speed limitations. Another group of topologies [14–19] uses P- and N- channel MOSFETs, can operate up to 60 MHz and produce long pulse trains; it poses low intrinsic losses but is not able to produce high voltage excitation (maximum 240 Vp–p).

Transformer push–pull topology offers an efficient MOSFET drive, can achieve high frequencies, offer low intrinsic losses but the lower end of operation frequencies is limited to 0.5 MHz [20,22].

The aim of the presented design was to develop the pulser suitable for up to 500 Vp–p rectangular pulse trains generation into capacitive or resistive load over 1 kHz to 5 MHz bandwidth. Pulser output amplitude must be stable when the load is changed from light load (open or less than 500 pF) to highly capacitive (3000 pF) or 50 Ω [23]. It must ensure minimal losses when running under light loads.

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2. Pulser design

A conventional pulser (Fig. 1) contains one switch to produce the leading edge and resistor pull-up to produce the trailing edge [1,2]. The circuit is extremely simple: leading edge of the pulse is steep and produces wideband response. Therefore, such excitation circuit became a standard in ultrasonic equipment.

This topology is not suitable for pulse trains generation: pull-up resistor value has to be decreased in order to get fast response for trailing edge. Then it will consume large power when the switch is on. Such losses can be tolerated when the pulse duration is short. As it was mentioned above, the pulser is aimed for high voltage excitation from 5 MHz down to 1 kHz. Consequently, topology with two active elements is needed. One element is responsible for pulling up (positive pulse) and another element should pull down [13].

2.1. Topology selection

Driving of the low side MOSFET is easy: a variety of suitable N-channel MOSFETs and the corresponding drivers exists. The problem lies in driving the high side switch. Transformer push–pull topology is a suitable solution since both MOSFETs are N-channel and are referenced to ground [20,22]. Unfortunately, the transformer size can become large here if operating frequencies below 1 MHz are required.

The most attractive solution for a high side drive is to use P-channel MOSFET. The main advantage of P-channel MOSFET is the simplified gate drive topology for high-side switch. The main disadvantage of this device is a high drain–source resistance $R_{ds(on)}$ in comparison with the N-channel device. Also, the device switching speed is low due to increased gate charge. Circuits for coded excitation using P- and N-channel MOSFETs have been suggested [14,15] for small transducers (i.e. phased array) and voltages below 100 V. Yet, higher voltages and longer pulse trains with high current output are needed for the tasks discussed above.

Half bridge (totem-pole) topology using two N-channel MOSFETs was suggested in [13] for frequencies below 1 MHz. This design uses a floating high-side driver IC which is commercially available. Unfortunately, commercial high side coupling circuits are slow: the propagation delay is more than 100 ns [13]. Though suitable for low frequency ultrasound [21], upper operation frequency of such circuitry is limited to a few MHz. Better results are obtained when transformer gate drive is used in half bridge topology [24]. However, transformer magnetising inductance limits the lower frequencies. Increasing the magnetising inductance is not the solution since this would increase the leakage inductance hence the upper achievable frequencies. The circuit suggested in [25] allows for higher pulse durations using diode and additional transistor. Unfortunately, such circuit would increase the available gate pull-down impedance hence the dV/dt immunity of the output MOSFET [26]. The half bridge pulser presented in [27] was able to achieve 2.7 MHz operation. Again, limitation is the speed of the high side MOSFET driver. Nevertheless, half bridge topology seems the suitable topology if frequencies below 1 MHz are considered.

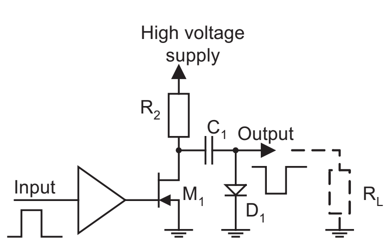

Fig. 1. Conventional pulser topology with one active element.

But existing commercial high side drivers are slow and do not offer significant gate drive current to achieve dV/dt immunity [26] and high speed switching.

2.2. Circuit design

Half bridge topology was proposed for the pulser (Fig. 2). It must be noted that driving of the high side switch is complicated: source of the N-cannel MOSFET floats at a high slew rate. A special high speed driver and floating +12 V power supply have to be derived. The novelty of the approach is that a high-speed digital isolator ISO721 (50 V/ns maximum slew rate) was used to deliver the logic signal into the floating high side driver. Another improvement is that the bootstrapped [13] power supply was replaced by an isolated DC/DC converter LME1212SC to ensure down to DC operation of the pulser.

Two IXFH10N80Q N-channel 800 V power MOSFETs were used as low and high side switches. This MOSFET has 30 A peak drain current I_{Dpeak} and 1.1 Ω R_{DS}. Such current according to [13] is sufficient to ensure 11 MHz maximum operating frequency for 3000 pF load. The resistance in the switch path can be up to 6 Ω because it is the current that mostly defines the ramping speed. Resistors R2 and R1 were added to further decrease the d*i*/d*t* stress on MOSFETs and reduce the output ringing. The actual operating frequency will be lower due to the limitations in the driving circuitry and MOSFET interaction.

A high-speed MOSFET driver EL7155CS was used. This type of driver has separate sourcing and sinking outputs which are essential to keep the MOSFET dV/dt immunity and switching speed.

Half bridge is well known in motor drive and switched mode power supply applications where the load is inductive. The dead time between the turn on and turn off is inserted in order to reduce the cross-conduction losses here. This mode is addressed as zero voltage switching [28]. Application of the half bridge in the ultrasonic pulser is different since the load is usually capacitive. Output voltage remains on drain–source clamps due to the capacitive load. In case of the inductive load the inductor current is responsible for the removal of the remaining carriers from the drain–source channel of the MOSFET which is being turned off. In analysed case, this charge remains even under light load or open condition and has to be consumed by complementary MOSFET which is being turned on. Unintentional dV/dt turn-on of the not conducting MOSFET can occur if ramping is too fast.

The sink output of the driver was directly connected to the gate to ensure the dV/dt immunity. The sourcing output was connected through resistor *R*3, *R*4 in order to limit the slew rate of the MOSFET to the specified dV/dt.

Additional dead time was envisaged for high side and low side MOSFET drive in order to ensure that MOSFET gate is biased to switch off before the turn-on of the opposing switch. Driving signals were derived in CPLD (Complex programmable logic device) M4A3. Dead time between gate driving pulses [20] was introduced using internal gate delay.

The approximate cost of the components (printed circuit board and enclosure box excluded) is 47 EUR which is significantly less than the cost of the commercial pulsers. The size of the printed circuit board is 100 × 65 mm.

3. Experimental investigation

The pulser was manufactured according to Fig. 2 and an investigation of the performance was carried out. The experimental investigation included PSPICE simulation (OrCAD PSpice A/D 9.1).