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Simulation of dark current suppression in p–i–n InGaAs photodetector with $In_{0.66}Ga_{0.34}As$/InAs superlattice electron barrier

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HIGHLIGHTS

- We established a model for the photodetector with superlattice electron barrier.
- We analyzed the electrical characteristics of photodetector by simulation.
- The superlattice period versus dark current was primarily studied.

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ABSTRACT

An InGaAs–based photodetector with different periods of inserting strain–compensated $In_{0.66}Ga_{0.34}As$/InAs superlattice (SL) electron barrier in the $In_{0.83}Ga_{0.17}As$ absorption layer has been investigated. The band diagram, electron concentration and electric field intensity of the structure were analyzed with numerical simulation. It was found that the period of SL has a remarkable influence on the properties of the photodetectors. With the decrease of the period of $In_{0.66}Ga_{0.34}As$/InAs SL, the dark current density is suppressed significantly, which is reduced to 2.46×10^{-3} A/cm^2 at 300 K and a reverse bias voltage of 1 V when the period is 2.5 nm.

1. Introduction

Extended wavelength $In_xGa_{1-x}As$/InP photodetectors (PDs) in the near infrared (NIR) range have attracted much more attention due to their importance in remote sensing such as earth observation, environmental research, and special night version [1–3]. Dark current is a key performance parameter for the devices. In general, there are four main contributions to dark current in PDs based on narrow band gap semiconductors: surface current associated with the surface states in the junction (I_{SURF}); generation recombination current associated with the Shockley–Reed–Hall process in the depletion region (I_{SRH}); trap-assisted current associated with tunneling effect in different barriers (I_{TAT}) and diffusion current associated with Auger or radiative processes in the extrinsic area (I_{DIFF}) [4]. The increase of Indium composition ($x > 0.53$) usually leads to lots of defects owing to the lattice mismatch between $In_xGa_{1-x}As$ layer and InP substrate, influencing the device performance. Improving material quality and growth conditions is a traditional and effective way reducing the dark current. P–i–n structure is commonly used for InGaAs–based PDs due to high quantum efficiency and short response time [5–8]. Recently, energy band engineering has been proposed, which suppresses dark current by tailoring the carriers transport optionally. Maimon et al. presented a nBn structure detector and reduced the dark current significantly by eliminating the I_{SRH}, however, no strain compensation was introduced to lower the I_{SURF} [9–11]. Gu et al. proposed a strain-compensated $In_{0.66}Ga_{0.34}As$/InAs superlattice (SL) electron barrier in metamorphic $In_{0.83}Ga_{0.17}As$ PDs [12], results show that the dark current was reduced dramatically compared with the conventional methods, and the photo-current is almost unaffected by the inset SL. But the period is fixed at 10 nm for each SL. And reports involving the influence of SL period on dark current is rather limited.

In this work, the effective dark current suppression has been presented with a proper control over SL period. Band diagram and electron concentration are analyzed systematically. The electric field intensity versus different SL period was then primarily studied in order to comprehend the behavior of $In_{0.66}Ga_{0.34}As$/InAs SL reducing dark current. All these electrical properties were investigated numerically with Silvaco software [13].

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2. Simulation and discussion

As shown in Fig. 1, the 2D structure of the detector with an inserted SL (hereafter PD–1) used in our simulation consists of a 200 nm InP substrate, 100 nm $In_{0.52}Al_{0.48}As$, 1900 nm $In_yAl_{1-y}As$ continuously graded buffer layers (n^+, 1×10^{18} cm^{-3}, y was graded from 0.52 to 0.87), 72 nm $In_{0.83}Al_{0.17}As/In_{0.83}Ga_{0.17}As$ interface digitally graded superlattice (DGSL), 700 nm $In_{0.83}Ga_{0.17}As$ absorption layer (n^-, 3×10^{16} cm^{-3}), a $In_{0.66}Ga_{0.34}As$(5 nm)/InAs(5 nm) SL with 10 periods, 700 nm $In_{0.83}Ga_{0.17}As$ absorption layer (n^-, 3×10^{16} cm^{-3}), followed by a 72 nm $In_{0.83}Ga_{0.17}As/In_{0.83}Ga_{0.17}As$ interface DGSL and 530 nm $In_{0.83}Ga_{0.17}As$ cap layer (P^+, 2×10^{18} cm^{-3}). A reference photodetector without the SL (hereafter PD–2) was also built. In our simulation, some special physical models for bipolar device were selected: temperature dependent analytic model, concentration dependent mobility model, trap-assisted tunneling (TAT) model, auger recombination model and band-to-band tunneling model. The main parameters at 300 K used in the simulation are listed in Table 1.

Fig. 2 presents the simulated Current–Voltage (I–V) characteristics at T = 275, 300 and 325 K along with the experimental data in Ref. [12]. When the reverse bias lower than 0.2 V, the measured dark current is around the lowest limitation of the measurement system [12]. So, the real dark current should be lower than the experimental data, and it is found that the dark current decreases monotonically with temperature for PD–1 and PD–2. But the dark current of PD–1 is obviously lower than those of PD–2 at the same temperature. For the temperature at 275, 300 and 325 K, the simulated dark currents of PD–1 are 1.22 μA (6.22×10^{-4} A/cm^2), 6.39 μA (3.26×10^{-3} A/cm^2) and 31.85 μA (1.62×10^{-2} A/cm^2) at a reverse bias voltage of 1 V, respectively. However, the simulated dark currents of PD–2 are 2.25 μA (1.14×10^{-3} A/cm^2), 10.85 μA (5.52×10^{-3} A/cm^2) and 51.31 μA (2.61×10^{-2} A/cm^2) at the same bias voltage, respectively, so PD–1 has a decreasing rate of 184%, 169% and 161% as a reference for PD–2. The dark current suppression is mainly owing to the decrease of electron flow, which was blocked by the $In_{0.66}Ga_{0.34}As$/InAs SL, meaning the n (electron concentration) is reduced in Eqs. (1) and (2) for PD–1, leading to a smaller SRH and TAT electron generation rate for PD–1 compared with PD–2.

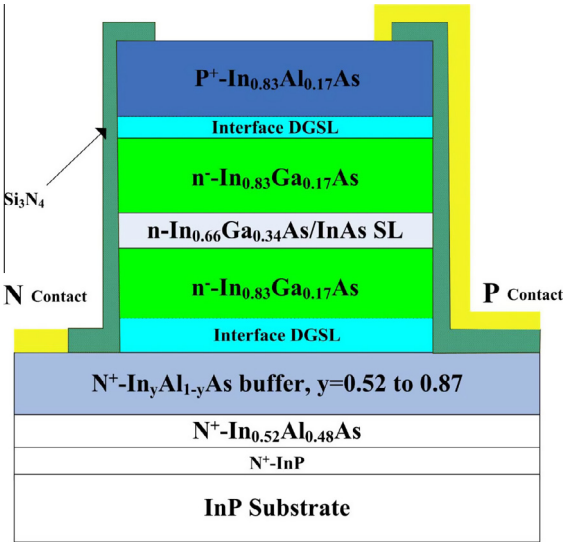

Fig. 1. Schematic mesa–type photodetector structure with an inserted SL.

Table 1
Parameter values used for In0.66Ga0.34As/InAs SL in metamorphic $In_{0.83}Ga_{0.17}As$ PDs in Silvaco simulation at 300 K.

Parameter	Value ($In_{0.83}Ga_{0.17}As/In_{0.66}Ga_{0.34}As$/InAs)
Band gap E_g (T = 300 K)	0.48, 0.62, 0.36 eV
Parameter	13.9, 13.2, 14.5 ε_0
Electron affinity	4.70, 4.56, 4.9 eV
Electron effective mass	0.025, 0.04,0.025 m_0
Lifetime (T = 300 K)	100, 100, 10 ns
Electron mobility	3500, 3000, 4000 cm^2/v s
Hole mobility	250, 200, 450 cm^2/v s

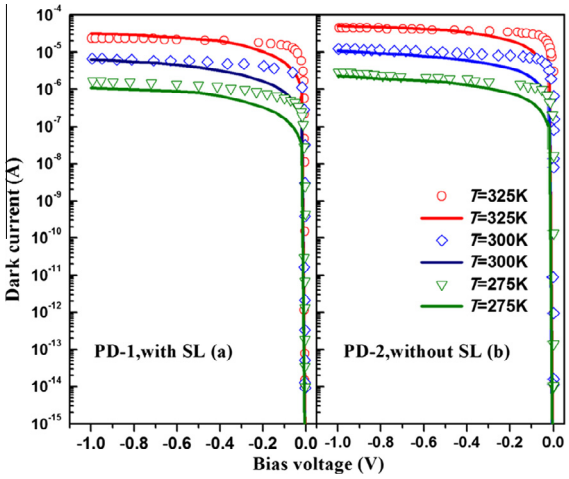

Fig. 2. I–V characteristics of simulated data (solid line) and experimental data in Ref. [12] (circles, rhombus and triangles) of (a) PD–1 and (b) PD–2 at T = 275, 300 and 325 K.

In our simulation, SRH generation rate of carriers is defined as

$$R_{SRH} = \frac{N_T(pn - n_i^2)}{\tau_{p0}\left[n + n_i \exp\left(\frac{E_i - E_T}{kT}\right)\right] + \tau_{n0}\left[p + n_i \exp\left(\frac{E_T - E_i}{kT}\right)\right]} \quad (1)$$

where τ_{p0} and τ_{n0} are the electron and hole lifetimes due to SRH processes, n_i and E_i are the intrinsic carrier concentration and intrinsic Fermi level, E_T and N_T are the trap level and trap concentrations, p is the hole concentration.

For dark current due to TAT process, the generation due to tunneling is given as

$$R_{TAT} = \frac{N_T(pn - n_i^2)}{\frac{\tau_{p0}}{1+\Gamma_p^{DIRAV}}\left[n + n_i \exp\left(\frac{E_i - E_T}{kT}\right)\right] + \frac{\tau_{n0}}{1+\Gamma_n^{DIRAV}}\left[p + n_i \exp\left(\frac{E_T - E_i}{kT}\right)\right]} \quad (2)$$

Here Γ is given by

$$\Gamma = \frac{\Delta E_T}{kT}\int_0^1 \exp\left(\frac{\Delta E_T}{kT}u - \frac{4}{3}\frac{\sqrt{2m^*(\Delta E_T)^3}}{3qh|E|}u^{\frac{3}{2}}\right)du \quad (3)$$

where ΔE_T is related to trap level, kT is the thermal energy, q is the absolute value of the electron charge, h is the Planck constant, m^* is the tunneling effective mass of the carriers, $|E|$ is the absolute value of the electric field, and u is the integration variable. The details of *TAT* and *SRH* modeling are explained elsewhere [13,14].

Fig. 3 shows the simulated energy band diagram under reverse bias of 1 V. It is worth noting that the valence band offset ratio of the high–indium InGaAs/InAs heterostructure is much smaller than its conductive band offset ratio [15], which structure blocks the flow of majority carrier current (electron in this paper), while allowing the flow of minority carrier current (hole in this paper) [16] and the simulated contour map of electron concentration at T = 300 K, anode bias (V_A) at −1 V and SL period is 10 nm is shown